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Attorney Docket No.	503.38097X00
First Inventor or Application Identifier	Ryoichi KAJIWARA, ET AL.
Title	SEMICONDUCTOR DEVICE
Express Mail Label No.	

APPLICATION ELEMENTS

See MPEP chapter 600 concerning utility patent application contents.

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1. [X] * Fee Transmittal Form *(e.g., PTO/SB/17)* *(Submit an original and a duplicate for fee processing)*
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   - Descriptive title of the Invention
   - Cross References to Related Applications
   - Statement Regarding Fed sponsored R & D
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   - Background of the Invention
   - Brief Summary of the Invention
   - Brief Description of the Drawings *(if filed)*
   - Detailed Description
   - Claim(s)
   - Abstract of the Disclosure
3. [X] Drawing(s) *(35 U.S.C. 113)* [Total Sheets 22]
4. Oath or Declaration [Total Pages 3]
   a. [X] Newly executed (original or copy)
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TITLE OF THE INVENTION

SEMICONDUCTOR DEVICE

BACKGROUND OF THE INVENTION

The present invention relates to a semiconductor device, particularly, to a semiconductor package structure adequate for decreasing electrical resistance of semiconductor package without Si chip.

An example of conventional transistor package is disclosed in JP-A-8-64634 (1994). A semiconductor chip, whereon electronic circuits are formed, is bonded to a die pad for heat release at rear plane electrode side by welding. A bump is formed on Al electrode at circuit formed plane side of the chip, and an inner lead is connected electrically and mechanically thereon. An inner lead is also connected to the die pad, and the chip, the die pad, and a part of the lead is sealed with resin so as to cover them. In a case when the bump is solder, the lead side is plated with tin (Sn), gold (Au), or solder, and the like, and bonded with the bump by melting the solder of the bump. In a case when the bump is gold, the lead is plated with tin, and bonded with the bump by an Au-Sn eutectic reaction. The inner lead is composed of three lines for source electrode, drain electrode, and gate electrode, respectively. The lead for source electrode is manufactured in a comb teeth shape. A through opening to the resin is formed on the head.

JP-A-5-121615 (1993) discloses a surface mounting

type semiconductor package having a wireless structure as another conventional example. Three external connection terminals are connected to electrode terminals of the semiconductor chip. Two electrodes on upper surface of the chip are connected to the external connection terminals by thermocompression bonding of Au balls. Mounting on a circuit substrate is performed by soldering the tip region of the lead terminals, which are protruded forward and backward from the chip mounting portion, to the terminals of the substrate.

In accordance with conventional standard surface mounting type semiconductor package, the semiconductor chip is bonded to the die pad of the lead for drain by soldering, and the source electrode and the gate electrode of the semiconductor chip are connected to the leads for source and gate of the external connection terminals by Al wire bonding. The chip, respective lead, and a part of the die pad are molded with resin. The die pad is exposed at bottom of the resin body so as to make the structure of the resin body possible to be connected to circuit substrate, and its size is set as larger than the size of the resin mold.

In accordance with conventional chip die pad bonding structure of the semiconductor chip, a bonding structure by a resin with conductive particles, wherein Pb rich solder having a low yield strength or Ag particles are mixed, has been adopted in order to prevent the chip from generating a high stress when the chip is fixed to

a member made of Cu base alloy.

The electrical resistance of the semiconductor package without Si chip in the surface mounting type plastic package of conventional vertical semiconductor element has been from several tens mΩ to ten and several mΩ with a wire bonding structure. In accordance with advancement of semiconductor technology, on-resistance of the element has been decreasing year by year, and at present, a device of several tens to several $m\Omega/cm^2$ has been developed. Further decrease of the resistance can be expected in future. In that case, decrease of the electrical resistance of the semiconductor package without Si chip is indispensable for improving the performance of the semiconductor package, because the electrical resistance of semiconductor package without Si chip becomes larger than device resistance. An prior art regarding the on-resistance of the semiconductor package is disclosed in JP-A-8-64634. The prior art is proposed relating to an insert mounting type package. The insert mounting type package is not restricted in size, and a thick and large size die pad can be used, because the bonding between the substrate and the lead is strong structurally. Therefore, decrease of the electrical resistance of semiconductor package without Si chip is relatively easy. However, the surface mounting type package has a property that a fatigue strength of the bonding portion is weaker than that of the insert mounting type package, because it has a structure that tip of the leads protruded from both

sides of the resin body is bonded to the terminal of the substrate by soldering two planes of small area each other. Therefore, it is necessary to absorb thermal strain between the package and the substrate accompanied with heat generation of the chip by deformation of flexible leads. Accordingly, it is necessary to make the shape of the leads thin and slender. In this case, decrease of the electrical resistance of semiconductor package without Si chip is difficult, because the electrical resistance of the lead itself is large.

In case of the surface mounting type package, the above problem can be solved by adopting a structure, wherein the die pad mounting the chip is soldered directly to the circuit substrate. However, if a position where the lead to be connected to the electrode at upper surface of the chip is protruded from the resin body differs in height from the position where the die pad is protruded, the contacting planes of the upper and lower metal molds for molding the resin becomes three dimensional structure, such a problem is raised that the manufacturing the metal molds becomes difficult. The above problem becomes significant when the lead frame is a matrix frame (arranged in X and Y directions) aiming at manufacturing a large number of the packages, simultaneously. The problem can be solved by making the size of the die pad small to be contained in the resin body, but if so, a pressing portion to press the die pad onto the bottom surface of the metal mold must be provided in the metal mold, in order to expose

the die pad at the lower plane of the resin body. If the size of the die pad is sufficiently large, it is possible to press the die pad onto the bottom surface of the metal molds. However, if the size of the die pad is as same as the size of the chip, the pressing portion can not be found on the die pad, and such a problem is raised that the die pad is molded with being exposed at the bottom of the resin body. Therefore, in case of the small size semiconductor package, wherein the size of the die pad is as same as the size of the chip, it is difficult to assembly the structure in such a manner that the die pad concurrently operating as the external connection terminals of the rear electrode is contained in the resin body.

On the other hand, conventionally, soldering connection or an adhering structure with a resin with conductive particles has been adopted for the connection of the rear plane of the chip with the external connection terminals such as die pad, and others. The soldering connection is superior connection structure in electrical resistance, thermal resistance, and heat resistance reliability. However, currently, in view of environmental problems, no use of Pb is required, and the conventional soldering material containing Pb must be replaced with new bonding material containing no Pb. There are various soldering material containing no Pb having a solidus line temperature below 250℃, but actually, there is no adequate soldering material containing no Pb having the solidus line temperature higher than 270 ℃,

which is durable against severe mounting on the substrate of the package. Exceptional only one material is Au-Si solder having the solidus line temperature of 370 ℃. However, Au-Si solder can not be adopted as the soldering material for the electrode at rear plane of the chip, by the two reasons such as a high cost and generation of cracks in the chip during cooling step after soldering when the size of the chip is large, because of a high yield strength. Therefore, a problem that practically there is no soldering material containing no Pb to replace the soldering material containing Pb is generated. On the other hand, adhesion with a resin with conductive particles is durable thermally in a short time against the necessary temperature for the mounting , i.e. 270 ℃, but weak in mechanical strength, because the adhesion strength is maintained by the resin. Even though tightness of the adhesion is reinforced with a shrinking force by curing the molding resin, the package having a large area or the package used in a high temperature has a problem that electric resistance and thermal resistance at the bonding portion are increased in accordance with deterioration of the resin, which is caused by change with elapsing time or temperature cycles. In particular, because the one plane molding structure, wherein the die pad (external connection terminals) is exposed to the surface of the resin body, is a structure which can not obtain the pressing force of the molding resin at the rear plane of the chip, a problem is raised that the long term reliability of the resin with conductive

particles adhesion portion is further decreased.

SUMMARY OF THE INVENTION

The present invention has been achieved in consideration of the above problems, and aimed at providing a semiconductor device comprising a package structure which can decrease electrical resistance of semiconductor package without Si chip.

The semiconductor device in accordance with the present invention is provided with a semiconductor element, which comprises a semiconductor substrate, a first electrode provided at the front plane of the semiconductor substrate, and a second electrode provided at the rear plane of the semiconductor substrate. A first metallic member is connected to the first electrode of the semiconductor element via a first metallic body containing a first precious metal , and a second metallic member is connected to the second electrode of the semiconductor element via a second metallic body containing a second precious metal .

In accordance with the present invention, the electrical resistance of the semiconductor package without Si chip can be decreased, because the first and second members are connected to the electrodes of the semiconductor element via the metallic bodies containing precious metal s, respectively.

In accordance with the above composition, the surface portion of the first metallic member and the

surface portion of the second metallic member for connecting to the external wiring are desirably positioned in an approximately same plane. The approximately same plane means, for instance, a plane of wiring substrate or circuit substrate of various electronic devices, whereon electronic members are mounted. Accordingly, the semiconductor device can be mounted by plane onto the wiring substrate or the circuit substrate.

As the first metallic body, there is an protrusion electrode protruded from the first electrode or the first metallic member of the semiconductor device. As the protrusion electrode, there are bump electrodes, or ball electrodes made of precious metal such as gold (Au) or silver (Ag), and others can be used. In order to decrease the electrical resistance of semiconductor package without Si chip, plurality of the protrusion electrodes are desirably arranged with an approximately same interval each other on whole surface of the bonding interface of the first electrode with the first metallic member.

As the second metallic body, a metal layer positioned at the bonding interface of the second electrode with the second metallic member can be used. The metal layer is desirably composed by bonding the respective of the precious metal layers positioned at bonding front plane sides of the second electrode and the second metallic member, respectively. As the material of the precious

metal layer, a precious metal selected from a group consisting of gold (Au), silver (Ag), platinum (Pt), palladium (Pd), and the like, or an alloy containing the above element as a main component can be used. A layer composed of plural kinds of precious metal s, or multi-layers of the alloy layer is also usable. Furthermore, any of the bump electrode or ball electrode made of precious metal such as gold (Au) or silver (Ag); silver (Ag) particles mixed with resin; a silver (Ag) member in a shape of plate, sheet, or network; and a silver member shaped in plate or sheet having bumps and dips, or cavity portions thereon; may be interposed between the precious metal layer positioned at the second electrode side and the precious metal layer positioned at the second metallic member side. As the desirable other metal layer, an alloy layer containing precious metal as a main component, of which solidus line temperature is higher than 400℃, is usable. As the material of the alloy layer, an alloy of silver (Ag) and tin (Sn) containing silver as the main component can be used.

A precious metal layer may be provided on the bonding surface of the first and second electrodes, and of the first and second metallic members of the semiconductor device. As the material of the above precious metal layer, a precious metal selected from a group consisting of gold (Au), silver (Ag), platinum (Pt), palladium (Pd), and the like, or an alloy containing the above element as a main component can be used. As the

material of the first and second electrodes of the semiconductor device, aluminum, or an aluminum alloy such as aluminum-silicon can be used.

The first and second metallic members connect electrically the first and second electrodes of the semiconductor element to external electrodes, wiring substrate, circuit substrate, and others. For instance, the first and second metallic members are lead wire, lead electrodes, or die pad terminals, which are a part of the semiconductor package, and others, or a part of these members. In order to decrease the electrical resistance of semiconductor package without Si chip, the first metallic member desirably comprises plural portions extending from the portion having the bonding portion with the first electrode, and respective of the plural portions comprises a surface portion for connecting with external wiring. In accordance with the circuit substrate or wiring substrate connecting to the semiconductor device, respective of the surface portion as described above of the first metallic member is provided with a conductor portion (for instance, copper foil) for electrical connection. The conductor portions are connected electrically on the circuit substrate or the wiring substrate. For instance, a continuous conductor (for instance, copper) pattern can be used as the conductor portion of the printed substrate.

The composition of the semiconductor device in accordance with the present invention as described above

can be applied to semiconductor devices, wherein the semiconductor element and the first and second metallic members are coated with an insulating material, such as the resin sealing type or resin molding type semiconductor devices. In these cases, the rear plane of the bonded plane of the first metallic member bonded with the first electrode has desirably an exposed portion for connecting with external wiring. In addition to the above composition, the bonded plane side of the semiconductor element is used as a circuit forming plane (for instance, a plane whereon one of main current electrodes and a control electrode of the vertical semiconductor switching element are formed), and the first electrode is desirably used as the main current electrode. In accordance with the semiconductor device, wherein the semiconductor element and the first and second metallic members are coated with an insulating material, the rear plane of the bonded plane of the second metallic member bonded with the second electrode may have the exposed portion for connecting with external wiring. As the insulating material, ceramics and other insulators can be used, in addition to various resins.

The various composition described above can be used concurrently. However, some compositions have a function and an advantage to decrease the electrical resistance of semiconductor package without Si chip by itself, such as the other semiconductor device of the present invention described hereinafter.

As the other semiconductor device of the present invention, the semiconductor package, which contains the semiconductor element comprising the first electrode and the second electrode on the front plane and the rear plane of the semiconductor substrate respectively, can be composed by any one of the following composition:

1) A composition, wherein the second electrode and the second metallic member are bonded via a metallic layer; the metallic layer is composed by bonding precious metal layers, one of which is provided on the bonding front plane of the second electrode, and another one of which is provided on the bonding front plane of the second metallic member.

2) A composition, wherein the second electrode and the second metallic member are bonded via an alloy layer; the alloy layer is composed of an alloy containing precious metal as a main component, of which solidus line temperature is higher than 400 ℃.

3) A composition, wherein the first metallic member comprises plural portions extending from the bonding portion with the first electrode, and respective of the plural portions comprises a surface portion for connecting with external wiring.

The composition of 1) or 2), and the composition 3) can be used concurrently.

Respective of the semiconductor devices of the present invention described above can be applied to various semiconductor element such as MOS (Metal Oxide

Semiconductor) field effect transistor, MIS (Metal Insulator Semiconductor) field effect transistor, bipolar transistor, insulated gate bipolar transistor, diode, or integrated circuits, and the like. The composition of respective of the semiconductor devices of the present invention is preferably applied to the semiconductor element, wherein the first electrode and the second electrode are used as a pair of main current electrodes; and to the vertical type semiconductor element such as power MOSFET and power transistor, wherein the first and the second electrodes are used as the main current electrodes, and the main current passes vertically in the semiconductor substrate in a direction from the first electrode at the front plane side to the second electrode at the rear plane side, or in a reverse direction. In this case, on-resistance, or on-voltage between the terminals including the package can be decreased, accompanied with low on-resistance characteristics of the semiconductor element.

In accordance with the semiconductor device of the present invention, the bonding strength of the Au bump/Al electrode bonding portion is improved by changing the Al film between the Au bump/Si substrate to an Au-Al compound in all the thickness direction of more than 80 % of the bonding area by heating treatment of the Au bump/Al electrode bonding portion at a high temperature. Furthermore, the temperature cycle life is improved by forming a structure, wherein a compression load is added

to the bonding portion by filling the resin between the electrode lead and the chip.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a set of drawings indicating an embodiment of the semiconductor package of the present invention,

FIG. 2 is a drawing indicating another embodiment of the semiconductor package of the present invention,

FIG. 3 is a drawing indicating another embodiment of the semiconductor package of the present invention,

FIG. 4 is a set of drawings indicating another embodiment of the semiconductor package of the present invention,

FIG. 5 is a drawing indicating an embodiment of the lead frame using for the semiconductor device of the present invention,

FIG. 6 is a drawing indicating an embodiment of the assembled structure and assembling method of the semiconductor package of the present invention,

FIG. 7 is a drawing indicating an embodiment of the lead frame structure under assembling the semiconductor package of the present invention,

FIG. 8 is a drawing indicating an embodiment of the resin molding method for the semiconductor package of the present invention,

FIG. 9 is a drawing indicating an embodiment of the assembling flow of the semiconductor package of the present invention,

FIG. 10 is a set of drawings indicating an embodiment of the assembled structure of the semiconductor package containing no Pb of the present invention,

FIG. 11 is a set of drawings indicating an embodiment of the semiconductor package containing no Pb of the present invention,

FIG. 12 is a set of drawings indicating an embodiment of the bonding member containing no Pb of the electrode at the rear plane of the chip of the present invention,

FIG. 13 is a drawing indicating another embodiment of the bonding member containing no Pb of the electrode at the rear plane of the chip of the present invention,

FIG. 14 is a set of drawings indicating another embodiment of the bonding member containing no Pb of the electrode at the rear plane of the chip of the present invention,

FIG. 15 is a drawing indicating another embodiment of the semiconductor package of the present invention,

FIG. 16 is a drawing indicating another embodiment of the semiconductor package of the present invention,

FIG. 17 is a drawing indicating another embodiment of the semiconductor package of the present invention,

FIG. 18 is a drawing indicating an embodiment of the wiring substrate mounting the semiconductor package of the present invention,

FIG. 19 is a drawing indicating an embodiment of the electronic device mounting the semiconductor package of the present invention,

FIG. 20 is a drawing indicating a current path model of the semiconductor package,

FIG. 21 is a set of drawings indicating a fundamental structure of the semiconductor package of the present invention,

FIG. 22 is a set of drawings indicating an embodiment of the structure of the transistor package of the present invention,

FIG. 23 is a drawing indicating another embodiment of the structure of the transistor package of the present invention,

FIG. 24 is a drawing indicating another embodiment of the structure of the transistor package of the present invention,

FIG. 25 is a drawing indicating another embodiment of the structure of the transistor package of the present invention,

FIG. 26 is a drawing indicating an embodiment of a cross sectional structure of the die pad-bonding film of the present invention,

FIG. 27 is a drawings indicating another embodiment of a cross sectional structure of the die pad-bonding film of the present invention,

FIG. 28 is a set of drawings indicating an embodiment of the bonding method using the die pad-bonding film of the present invention,

FIG. 29 is a graph indicating an experimental data on the relationship between the strength of Au/Al bonding

portion versus the holding time at a high temperature,

FIG. 30 is a graph indicating an experimental data on the relationship between the strength of Au/Al bonding portion versus the holding time at a high temperature,

FIG. 31 is a drawing indicating an embodiment of alloying the bump of the front plane side electrode with a metal having a low melting point,

FIG. 32 is a drawing indicating an embodiment of mounting the semiconductor package shown in FIG. 31 onto the wiring substrate,

FIG. 33 is a drawing indicating an embodiment of mounting the semiconductor package of the present invention omitting the die pad onto the wiring substrate,

FIG. 34 is a drawing indicating an embodiment of mounting the plane mounting type semiconductor package of the present invention onto the wiring substrate,

FIG. 35 is a drawing indicating a semiconductor element using for assembling the semiconductor package of the present invention.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

The first embodiment of the present invention is a structure assembled by the steps of: connecting directly a gate electrode and a source electrode of transistor chip to a metallic member for external connection (lead) via plural Au bumps arranged in the optimum manner; connecting electrically and thermally a drain electrode at the rear plane of the chip to the metallic member for external

connection (die pad) to make the source electrode and any one of the metallic member for the gate electrode (lead) or the metallic member for the drain electrode (die pad) contain into internal of a polyhedral package. In accordance with the above structure, the planes of the metallic member contained in the package can be bonded by soldering to a terminal plane of a wiring substrate. Desirably, the structure is assembled so as to extend tips of the leads or the die pad from the two side planes of the package, and to make it possible to press the metallic member contained in the package onto the bottom plane of the metal molds via the metallic member protruded from the package.

The second embodiment of the present invention is a structure, wherein the drain electrode is bonded to the precious metal plated metallic member (die pad) via any one of precious metal bumps, a mesh sheet made of precious metal , precious metal particles, a thick precious metal plating having a hardness less than 60 Hv directly, or via an alloy layer having a solidus line temperature at least 400 ℃, which contains a precious metal as a main component. The bonding portion can be obtained by compression bonding using heating and ultrasonic vibration. Desirably, when the chip size is large, the structure is assembled by forming the Au bumps onto the source electrode and the gate electrode on the circuit forming plane of the chip, and bonding the electrodes directly to the lead plated with precious metal .

Furthermore, the structure is assembled so that the size of the lead at the source electrode side is made equal to the size of the die pad at the rear plane of the chip, and the members are arranged symmetrically, in order to prevent the chip from adding a bent stress.

The third embodiment of the present invention is a structure and a method for assembling the structure by the steps of: forming previously a large number of Au bumps onto the source electrode and the gate electrode made of Al on the chip; mounting the chip aligned to respective of the leads plated with precious metal ; mounting a precious metal member having a smaller hardness than the Au bump thereon; mounting a die pad plated with precious metal thereon; and bonding all the contacting boundary planes simultaneously with heating, loading, and ultrasonic vibration by arranging a bonding tool, which gives pressure and ultrasonic vibration, on the die pad.

The first embodiment is explained in detail hereinafter.

A current path model of the semiconductor package is indicated in FIG. 20. Respective of the reference marks indicates the following members.

184: external connection terminal for drain,

186: bonding portion,

182: electrode at the rear plane of the chip,

180: chip,

181: Al electrode,

185: metallic bump, and

183: external connection terminal for source (lead).

The electric resistance R between the external connection terminals for source and the external connection terminals for drain is expressed by the following equation (1):

$$R = R1 + R2 + R3 + R4 + R5 + R6 + R7 \quad \ldots(1)$$

The part obtained by eliminating the internal resistance of the chip R4 from the equation (1) can be regarded as the electrical resistance of semiconductor package without Si chip. The resistance of the bump R6 can be expressed by the following equation (2):

$$R6 = (\rho \times h/S)/n \quad \ldots(2)$$

where,

ρ : specific resistance of the bump

h : height of the bump

S : cross sectional area

n : number of the bumps

The regular size of the Au bump is 150 μm in diameter and 20 μm in thickness, if the Au bump is formed by a ball bonding method of wire, which makes it possible to form the bump directly on the Al pad with low cost. The resistance of the bump in the above case becomes (0.026/n) mΩ of sufficiently small. The resistance R5 of the Al

electrode film can be expressed by the following equation (3):

$$R5 \fallingdotseq (\rho/4\pi t)\ \ln(r2/r1) \qquad \ldots(3)$$

where,

ρ : specific resistance of the electrode film

t : thickness of the electrode film

r2 : the outer diameter of the electrode

r1 : the diameter of the bump

The outer diameter of the electrode is approximately proportional to $1/(n^{1/2})$ when n pieces of the bumps are arranged uniformly. Therefore, if the n is increased, the r2/r1 comes to close 1, and the R5 can be decreased sufficiently by increasing the thickness of the electrode film and the number of the bump. The resistance of the external connection terminals (R1 + R7) can be expressed simply as the following equation (4):

$$(R1 + R') = (\rho \times L/S) \qquad \ldots(4)$$

where,

ρ : specific resistance of the lead

L : current-carrying length of the lead

S : current-carrying cross sectional area

The resistance of the external connection terminals becomes approximately 1.4 mΩ in case of the regular SOP package for surface mounting (thickness: 0.16 mm, width:

0.3 mm, length: 2 mm x 2). That is, in a level that the electrical resistance of semiconductor package without Si chip is less than 1 mΩ, the electrical resistance of semiconductor package without Si chip can not be decreased only by adopting the bump structure, and the structure to decreased the resistance of the external connection terminals must be adopted.

Then, in accordance with the semiconductor device of the present invention, a structure is used, which ensures the reliability of the connecting portion of the external connection terminals with the wiring substrate in addition to decrease the resistance of the external connection terminals.

The fundamental structure of the semiconductor device 1 of the present invention is indicated in FIG. 21. The only one method to decrease the resistance of the external connection terminals is to increase the cross sectional area of the current path is increased and the length of the current path is decreased. Therefore, one of the external connection terminals has a structure to take the current path in the thickness direction of the terminal. In this case, the current-carrying cross sectional area is sufficiently large such as from several to several tens mm^2 in comparison with the current carrying distance (0.1 -0.2 mm), the resistance of the first external connection terminal portion 194 can be made less than 1 $\mu\Omega$. The other second external terminal portion 193 has a structure to connect with the terminal of the wiring

substrate by descending along the side plane of the chip, and the current-carrying distance becomes several millimeters. However, two times current-carrying cross sectional area can be ensured by using both sides of the package. In accordance with the present structure, a wide and thick member can be used as the second external connection terminal by the reason described later. Therefore, more several times current-carrying cross sectional area can be ensured, and the electric resistance can be decreased to approximately one-tenth in comparison with conventional package structure.

The conventional package structure has a problem that, if the rigidity of the second connection terminal is increased, the long term reliability at the connection portion with the wiring substrate is decreased. However, in accordance with the structure of the present invention, the temperature cycle reliability can be ensured even if the rigidity of the second connection terminal is high by the reason below. The reasons are that the temperature difference from the substrate is small because the structure is composed so that the area of the first external connection terminal at the bottom of the resin body is sufficiently large, and the chip, i.e. a heat source, and wiring substrate are located close each other, and that thermal distortion is small because the connecting terminal is made of a copper alloy having a thermal expansion coefficient close to that of the substrate. Accordingly, the absolute value of the thermal distortion

generated at the connecting portion of the first and second connection terminals with the substrate is small. A pressing force is generated at the connecting portion of the second connection terminal and the substrate with increasing the temperature because of the difference in thermal expansion in a height direction of the resin body from the Cu member corresponding to folded legs, and based on this effect, the temperature cycle reliability is improved in comparison with conventional package, and the rigidity of the second connection terminal can be increased.

During the molding step for assembling the package indicated in FIG. 21, the first connection terminal member 194 can be pressed toward the bottom plane of the metal molds via the precious metal bump 195 by pushing down the second connection terminal with the side wall of the upper die. Accordingly, the package, wherein the connection terminals are certainly exposed at the bottom plane of the resin body, can be assembled without adding any special measures to the die. In this case, the particularly important point is that the second connection terminal member connected via the bump are protruded from both side planes of the resin body. In accordance with pushing down at both sides of the second terminal member, generation of inclination of the first terminal member and splitting off the bump can be prevented, and faultless resin molding having a high production yield becomes available. In accordance with a structure to push down at one side, a

moment is generated between the die contacting portion of the pushed down second terminal member and the lower die contacting portion of the first terminal member. Then, the bonding portion is split off by generation of a tensile stress at a part of the bump bonding portion, and a failure that the resin is flown into the bonding plane is generated by separating one side of the first terminal member. Therefore, the faultless resin molding with a high production yield can not be ensured.

Then, the second embodiment is explained in detail. The characteristics required for bonding at the rear plane of the chip are four points as follows:

1) electrically conductive and thermally high-conductive to the external connection terminal (die pad),

2) long temperature cycle life,

3) durability against a soldering temperature at mounting the package onto the substrate, and

4) possibility to bond the wide area of the rear plane of the chip during a short tact in mass-production line with no undesirable influence.

Because no appropriate high melting point soldering material containing no Pb is available, the bonding satisfying the above characteristics must be achieved using materials other than soldering material. When precious metal material is used as the bonding material, thermal conductivity of the bonding material is approximately ten times of that of the soldering material. Accordingly, even if the bonding has a same thickness, the

same heat transfer characteristics can be obtained by one tenth of bonding area if the bonding portions distribute uniformly at the rear plane of the chip. That is, it is significantly advantageous in heat releasing characteristics.

Regarding the temperature cycle life, it is significantly influenced that what component can absorb thermal strain caused by difference of thermal expansion of the chip and the external connection terminal (die pad) by deformation. In accordance with conventional solder, most of the strain could be absorbed be deformation of the solder, because the yield strength of the solder is very low, and the destruction occurred at the soldering portion. In this case, the strain was scarcely transmitted to the chip, and there was an advantage that stability and reliability of the chip was maintained. On the contrary when the precious metal material is used for the bonding, the yield strength is higher than solder, and lower than Si and Cu. Accordingly, the strain of the chip and the die pad is increased, but life of the bonding portion is protruded. The amount of the strain added to the chip can be adjusted by providing cavities in the precious metal layer as much as the heat releasing characteristics does not have a serious problem. One of the practical measures to provide the cavities is using a mesh sheet, particles, or a sheet having dumps and dints as the bonding material.

Regarding heat resistance, there is no problem. The most important point is readiness of bonding and assembling.

When precious metal s were bonded each other by conventional thermocompression bonding method, it was necessary that the heating temperature was made in the range of 400-500 ℃, in order to bond in a short time. In accordance with this method, the amount of the thermal strain during the cooling step was large, because temperature difference from room temperature was significant, and a problem to have a large danger to cause destruction even in a case when the size of the chip is not remarkably large. In accordance with the present invention, a method has been adopted that the bonding temperature is specified as equal to or below 250 ℃ in order to solve the above problem, and ultrasonic vibration is utilized for achieving ensured bonding at the above temperature. However, when the chip is bonded to the die pad by thermosonic bonding method, a problem is generated that the chip is damaged at the portion where the circuit forming plane of the chip contacts with a hard bonding jig, because the ultrasonic vibration is added with compressing the die pad and the chip by holding them with a hard heating stage and a hard bonding jig. In accordance with the present invention, the above problem is solved by forming an Au bump onto the electrode at circuit forming side of the chip; arranging an external connection terminal member (lead) having the same size with the die pad at the circuit forming side; and forming a structure, wherein the chip does not contact directly with the hard bonding jig, in order to prevent the chip from being damaged. When the

bonding portions are provided at both upper and lower planes of the chip, respectively, generation of variation in bonding condition (a condition that one side is bonded tightly and another side is not bonded well) is concerned. However, in accordance with the ultrasonic vibration bonding method, if the bonding portions are arranged in series to the bonding jig, such a self adjusting function is operated that relative vibration at one portion is restricted in accordance with proceeding the bonding at the portion, and the relative vibration at the other portion, which is not bonded yet, is increased. Accordingly, the two bonding portions having approximately a same strength can be obtained. However, when the bonding area is desired to be enlarged at the rear plane of the chip in view of the heat release, it is possible to make a difference in the bonding areas by making the bonding materials at the upper plane and the rear plane of the chip different each other; and the bonding at the circuit forming plane side of the chip is performed with a bonding material having a higher yield strength, and the bonding at the rear plane side of the chip is performed with a bonding material having a lower yield strength. In accordance with adopting the above bonding structure and the bonding method, the bonding at the rear plane of the chip having high performance and high reliability becomes possible without using Pb.

The operation and the advantages of the third embodiment are as same as described in the second

embodiment. Practical bonding time is approximately several hundreds milliseconds except the time necessary for transferring and positioning the work, and is shorter than the time necessary for conventional plural wire bonding operation. It is necessary to form the Au bumps on the Al electrode of the chip, previously, but it does not influence to the production tact, and in view of a point that the chip-die pad connection and the bonding can be performed simultaneously, the production tact can be decreased in comparison with the conventional operation.

(EMBODIMENTS)

Hereinafter, practical structures of the above embodiments of the present invention are explained in detail referring to drawings.

FIG. 1 indicates an embodiment of the semiconductor package of the present invention. FIG. 1 (a) is a top plan view, FIG. 1 (b) is a cross sectional view, and FIG. 1 (c) is a bottom plan view. In accordance with the drawings, the semiconductor chip 1 is a vertical MOS transistor of 4 X 2 mm in size. The film thickness of the Al electrodes 2, 3 for source and gate is approximately 4 μm, and Au is vapor deposited onto the surface of the rear plane electrode 4, which is to be the drain electrode. A large number of or plural Au bumps 8 are formed onto the source electrode and the gate electrode of the chip by ball bonding method uniformly, that is, in a manner that the bumps are arranged with an approximately equal interval onto all the

surface of the electrodes. Respective of the lead terminals 5, 6, for the source and the gate has a structure, wherein the Cu core 11 is plated with precious metal 12 of Pd/Au, and its thickness is 0.2 mm. Width of the lead terminal for source 5 is approximately as same as the source electrode 2. That is, the lead terminal for source 5 covers almost all the surface of the source electrode 2. The Au bump on the chip and the Pd/Au plane of respective lead terminal is bonded directly by thermosonic thermocompression bonding method with heating at 230 ℃. The size of the Au bump bonded by the compression bonding method is approximately 120 μm in diameter and 40 μm in thickness. The external connection die pad terminal 7 has a structure, wherein the Cu core 13 is plated with precious metal 14 of Pd/Au, and its one plane is further plated with Ag 15 in approximately 10 μm. The Au plane of the rear plane electrode of the chip and the Ag plated plane of the die pad terminal is bonded directly by thermosonic thermocompression bonding method with heating at 230 ℃, as same as the case of the Au bump/lead terminal. The lead terminal for source is protruded outside from both left and right side walls of the molded resin body 16, and manufactured to be folded. The lead terminal having a wide width, which is protruded leftward and rightward, is provided with the slit 10 and some openings 9 at locations above the chip. The lead terminal for gate is also protruded outside from both left and right side walls of the molded resin body 16. The die pad terminal for drain

is exposed at the bottom of the resin body. The lower plane of the die pad terminal (a contacting plane with the connection terminal on the wiring substrate), and the lower planes (the same contacting plane) of the lead terminals for source and gate, which are manufactured to be folded, are manufactured to be a same height, that is, to be a same plane.

In accordance with the present embodiment, electrical resistance of semiconductor package without Si chip can be decreased significantly on account of its structure, wherein the source electrode and the lead terminals for source are connected by a large number of Au bumps arranged uniformly; the lead terminals having a wide width are protruded from both left side and the right side; the die pad terminals are connected directly to the rear plane electrode by the Ag plated film; the cross sectional area of the current path to the wiring substrate is large; and the conducting distance is very short (equal to only thickness of the substrate). Accordingly, a novel semiconductor device provided with an unprecedented semiconductor package having such a low electrical resistance of semiconductor package without Si chip as lower than 1 mΩ can be obtained. Additionally, an advantage such as the semiconductor package is superior in a long term reliability is realized, because the presence of the Au bumps of 40 μm in thickness on circuit plane and the Ag plated film of 10 μm in thickness on rear plane of the chip at the connecting portion of the chip

to the Cu terminal operates as a role of cushion material, because Au and Ag are soft material (yield strength are low) in comparison with the Cu terminal material, and an effect to prevent the chip from being influenced by a large force is realized; and Au and Ag have a longer temperature cycle life than that of solder. When the semiconductor package is mounted onto the wiring substrate, the package is bonded with the substrate via a wide area of the die pad terminal, and the chip, i.e. a heater, and the substrate are connected by the shortest distance under a preferable thermal conducting condition. Accordingly, the thermal strain generated between the substrate and the package is small, because the temperature difference between the package and the substrate is small, and the thermal expansion coefficient of the substrate and the thermal expansion coefficient of the Cu terminal are close each other. Therefore, such an advantage is realized that the connecting portion of the semiconductor package with the wiring substrate has a long temperature cycle life and a superior long term reliability. Furthermore, because the openings are provided at the lead terminal for source positioned above the chip, generation of voids in the resin molding step can be prevented by two effects such as entering the resin through the openings is generated and degassing through the openings are performed even if the Au bumps are flattened and the gap between the lead terminal and the chip is decreased. Accordingly, reliability of the package can be maintained.

A semiconductor package having a connecting structure of high heat resistance and high temperature cycle reliability can be provided, because thermosonic bonding of Au/Ag is performed via Ag plated film as the connecting structure of the rear plane electrode of the chip with the die pad terminal, which makes it solderless bonding.

Here, the size of the Au bump is made 120 μm in diameter. However, larger size of the bump such as several hundreds μm in diameter is desirable, if formation of the bump is possible. In accordance with increasing the size of the bump, the resistance can be further decreased, the bonding strength is increased, and such an advantage is realized that the production yield is increased, because generation of peeling off the bump bonding portion by an external force during assembly of the package can be prevented effectively.

FIG. 2 indicates an embodiment of the semiconductor package of the present invention, wherein the Ag bump compression bonding method is applied to the chip-die pad connection. In accordance with FIG. 2, the Al electrode 22 of the semiconductor chip 21 and the lead terminal 26 plated with precious metal 25 are bonded tightly each other via the Au bumps 30. The rear plane electrode 23 of the chip and the die pad terminal 29 plated with precious metal are bonded each other via the Ag bumps 31. The one side of the lead terminal is cut off at a portion near the side wall of the resin body 32, and the other side of the

lead terminal is manufactured to be folded and aligned at a same height as the die pad in order to connect with the terminals of the wiring substrate.

In accordance with the present embodiment, deformation can be absorbed structurally, because the chip and the die pad are connected by the Ag bumps. Therefore, the temperature cycle life at the bonding portion of the die pad terminal/chip is significantly long, and a semiconductor package containing no Pb, which is desirable in view of environmental problem, having a high reliability can be provided. The mounting reliability is improved significantly, because thermal strain is hardly added to the solder bonding portions of the connecting terminals of the wiring substrate. The size of the package can be decreased to an equivalent size as the chip, the thickness of the package can be decreased to approximately 1 mm, and a small size semiconductor package for surface mounting, which is appropriate for high density mounting, can be provided.

FIG. 3 indicates an embodiment of the semiconductor package of the present invention, wherein the Ag paste adhering method is applied to the chip-die pad connection. In accordance with FIG. 3, the Al electrode 36 of the semiconductor chip 35 and the lead terminal 40 plated with precious metal 39 are bonded tightly each other via the Au bumps 45. The rear plane electrode 37 of the chip and the die pad terminal 43 are adhered each other by the Ag paste 46. The die pad terminal has a structure, wherein

the Cu core 41 is plated with Pd/Au 42, and its peripheral planes are manufactured by counter boring in order to make an anchor effect operate to the molding resin. The lead terminals are protruded out from both sides of the resin body 47.

In accordance with the present embodiment, the same advantages as the embodiment indicated in FIG. 1 can be obtained. Because the peripheral planes of the die pad terminal are manufactured to be a shape which enables the die pad be engaged with the resin, the die pad terminal can be pressed to the rear plane of the chip by the shrinking force of the molding resin. Therefore, even if the chip/die pad connecting method by Ag paste, which makes the assembling readily, is adopted, a reliable semiconductor package can be provided.

FIG. 4 indicates an embodiment of the semiconductor package of the present invention, wherein the package structure enables the mounting of the circuit forming plane toward the wiring substrate. In accordance with FIG. 4, plural Au bumps 57 are formed on the Al electrodes 51, 52 for main current and for control on the circuit forming plane of the semiconductor chip 50, respectively, as same as the embodiment indicated in FIG. 1; and the external connection terminal for main current 55 and the external connection terminal for control 56, which are of the size equivalent to the size of respective electrode and containable in the resin body 59, are bonded thereon by thermosonic thermocompression bonding method. The

surface of the respective external connection terminal is plated by Pd/Au flush plating. The rear plane electrode 53, outermost surface of which is composed of Au or Ag vapor deposition film, is formed at the rear plane of the chip, and the external connection terminal 54 for rear electrode, Cu surface of which is plated by Pd/Au flush plating, is bonded thereon by thermosonic thermocompression bonding method interposing an Ag mesh sheet 58 plated with Sn of 0.1-5 μm in thickness between them. The external connection terminals for main current and for control are molded in a condition that they are exposed to the surface of the resin body, and the external connection terminals for rear plane electrode are protruded out from both left and right sides of the resin body. The one side of the external connection terminals for rear plane electrode is cut off, and the other side is manufactured to be folded.

In accordance with the present embodiment, the same advantages as the embodiment indicated in FIG. 1. Furthermore, cooling the package can be performed most effectively and the temperature rise at the Al electrode portion can be suppressed as small, because its structure enables the circuit forming plane of the chip, i.e. a heater of the chip, to release heat effectively to the wiring substrate. As the result, the product life under practical using condition can be improved significantly, because the thermal strain generated between the external connection terminals and the chip can be made small, and growing compounds between the Al electrode film and the

Au balls can be suppressed.

FIG. 5 indicates an embodiment of matrix lead frame for source and gate electrodes using for assembling the semiconductor package of the present invention, FIG 6 indicates the bonding method at assembling the package in view from the cross section A-A' in FIG. 5, FIG. 7 indicates an appearance of the matrix lead frame after bonding, and FIG. 8 is an illustration indicating the resin molding method. In accordance with FIG. 5, an unit, wherein the lead for source 61 and the lead for gate 62 make a pair to form the unit, is arranged in a X-Y direction. In accordance with next FIG. 6, the Au bumps 71 formed previously on the Al electrodes 66, 67 of the semiconductor chip are positioned and mounted onto the leads for the source 61 and for the gate 62 of the matrix lead frame. The die pad terminals 69 for drain, whereon the Ag bumps 70 are formed previously, are mounted onto the chip rear plane electrode 68. The bonding portions at the upper surface and the lower surface of the chip are bonded simultaneously by heating the heating stage 74 for mounting the matrix lead frame at 200 ℃, and compressing the die pad terminals by bonding tool 73, which gives ultrasonic vibration 76, with a force of 50 - 500 g per bump. In accordance with the ultrasonic vibration, the bonding operation is performed with controlling the flattened amount of the bumps, and preciseness of the height of the lead and the die pad is controlled to be within a designated range. The direction of the ultrasonic vibration is

restricted in the longitudinal direction (up and down direction in FIG. 5), where the rigidity of the lead is high, in order to prevent the bonding portion from generating bonding failure by resonance of the lead. The die pad terminal is manufactured by punching out from a large Cu plate which is plated previously with precious metal , because the die pad terminal is separated and assembled individually. The state wherein the matrix lead frame (FIG. 7) after completion of the bonding is set in a metal mold is indicated in FIG. 8. FIG. 8 indicates a cross sectional structure viewing from the direction perpendicular to the A-A' cross section in FIG. 7. In accordance with FIG. 8, the cavity 82 of the metal molds 80, 81 are formed matching with the arrangement of the matrix lead frame and arranging in the X-Y direction. Escaping spaces 83 for containing lead hangers are provided. The matrix lead frame is set into the cavity of the lower die 81 by positioning the semiconductor chip 65 so as to be contained, and then, the upper die is placed thereon and compressed. The height of the source and gate leads extending out from the cavity is adjusted to be equal to or somewhat higher than the depth of the cavity in the lower die, and its structure is composed so that, when the leads are held by the side walls of the upper and lower cavities, the die pad terminal is compressed toward the bottom of the cavity. The leads are pressed down at left and right as the chip portion is a center. However, if the amount of the pressing down is too large, the leads are influenced

by bending deformation, and an tensile stress is generated at the Au bump portion of the middle of the chip. Therefore, in order to make the bending deformation of the leads in a convex shape at the middle of the chip small as possible, the lead holding portion of the upper die is manufactured in a shape of knife, and the lower die is made to have a step, inner side of which is lower than the outer side, so as to deform the leads in a W-shape. Regarding the molding resin, size of the silica particles for lowering thermal expansion is decreased so as to improve the filling property into the gap of 10 - 20 μm between the bump bonding portion, in order to prevent generation of resin voids during the pressure-injecting process.

In accordance with the lead frame and the its manufacturing method, low cost semiconductor packages can be provided by the following effects: the IC units are arranged in matrix state in the lead frame for assembly, and productivity can be increased by increasing the number of packages taken from a lead frame; the die can be manufactured without increasing its cost, because the matching planes of the dies except the lead holding portions can be manufactured precisely by surface grinding manufacturing; decreasing the manufacturing steps is possible, because the die pad-chip connection, and the circuit forming plane side connection can be performed simultaneously by one bonding step; and others. Additionally, as a structural feature, a small and thin semiconductor package as small as close to the size of the

chip can be provided.

FIG. 9 indicates an embodiment relating to the assembling flow of the semiconductor package of the present invention. In accordance with FIG. 9, four components are used in assembling the semiconductor package. The semiconductor chip is provided with Au bumps, which are formed at wafer level, and cut pieces by dicing. Formation of the Au bumps can be performed by any one of the methods such as ball bonding method, plating method, and Au ball transcription method. The external connection terminals for source and gate are manufactured and reshaped by punching method or etching method from Cu alloy plate in a matrix lead frame shape, and after plating Ni onto the surface of the terminal as a base, Pd is plated by approximately 0.02 - 1 μm thick thereon. Finally, the terminals are finished by plating its outermost surface with Au of approximately 0.001 - 1 μm thick. The external connection terminals for drain is manufactured by plating surface of a Cu tape with Ni as a base, Pd is plated by approximately 0.02 - 1 μm thick thereon, the outermost surface of the terminals are plated with Au of approximately 0.001 - 1 μm thick, and finally, the Cu tape is cut to pieces of plates having an equivalent size to the chip. The Ag sheet for the chip-die pad connection is manufactured by forming the bumps and dips on one side or both sides of a Ag tape of 10-100 μm thick by pressing, and plating Sn of approximately 0.1 - 5 μm thick thereon. The thickness of the Sn at this time is determined so that

the weight ratio of Sn to Ag becomes equal to or less than 20 % by weight. Finally, the Ag sheet is cut to pieces of plates having an equivalent size to the external connection terminal for drain or the chip. Respective of the components are bonded simultaneously per one IC as an unit, after mounting the matrix lead frame onto the bonding stage, laminating in the order of the semiconductor chip, the Ag sheet, and the external connection terminals after positioning each other, and heating, pressing, and ultrasonic vibrating simultaneously. After finishing the bonding of all the matrix, the resin molding step is performed by the same procedure as the embodiment indicated in FIG. 8. Finally, the semiconductor packages connected in a matrix state are cut and separated to pieces, and the semiconductor package is completed by manufacturing the lead to fold and reshape.

In accordance with the present embodiment, manufacturing steps for the components can be performed in parallel lines, and an incorporated production of a large number of packages is possible; and the steps in the assembling line is only three steps such as (1) setting the components and bonding, (2) resin molding, and (3) cutting and reshaping the lead, and one step can be omitted in comparison with the conventional chip-die pad connection and the wiring bonding process. Furthermore, total production tact can be decreased, and significant improvement in the productivity can be realized, because the above step (1) in the tact for assembly can be performed

with less tact than the tact for wire bonding.

FIG. 10 indicates an embodiment of bonding structure of the chip rear plane electrode of the present invention. The lead frame is assembled with two lead frames such as the lead frame for source and gate, and the lead frame for drain. In accordance with FIG. 10, the lead frame made of Cu alloy forming the lead for source 91 and the lead for gate 92 , and the lead frame forming the die pad for drain 95 are plated with Pd/ Au all over the surface. The Au ball bumps 101 are formed on the die pad for drain by the ball bonding method. In accordance with this structure, the semiconductor chip 97 having the rear plane electrode 102, wherein the Au ball bumps 110 are formed previously on the Al electrode 98, is interposed between the above two kinds of lead frames, and the upper portion and the lower portion of the chip can be bonded simultaneously. FIG. 11 indicates an example of the semiconductor structure, which is obtained by molding the above bonded body with resin, and reshaping the lead. In accordance with FIG. 11, the source lead 91 and the gate lead 92 are protruded out from one side wall of the resin body 103, the lead for drain is protruded out from the other opposite side wall, and respective of the leads is manufactured by folding process. The neck portion 93, which means a locally slender portion, is provided to the leads in the resin body, in order to make the structure, wherein the stress generated at the folding process is hardly transmitted to the bonding portion of the bumps.

The height of the protruded position of the leads at left side differs from that at right side. Accordingly, the matching planes of the upper metal mold and the lower metal mold are manufactured with a step. The rear plane of the chip has a compression bonded structure of Au deposition film/Ag bumps 101/Pd/Au plated die pad, and the upper surface of the chip has a compressed structure of Al electrodes 98, 99/Au bumps 100/Pd/Au plated leads 91, 92.

In accordance with the present embodiment, a semiconductor package containing no Pb, which is desirable in view of environmental problem can be provided. Additionally, the heat resistance of the package is high because the chip-die pad structure is composed by direct bonding of precious metal s via the Ag bumps; and temperature cycle reliability of the package is high because thermal strain between the chip/die pad can be relaxed by the Ag bumps. The lead has a desirable wettability with solder. As the result, the assembling process of the package can be shortened and productivity is increased, because the solder plating after assembling the package becomes unnecessary. Additionally, such an advantage is realized that a small and thin semiconductor package can be provided, because the chip can be molded with resin in a size close to the chip size.

FIG. 12 indicates an embodiment of bonding sheet for bonding the chip and the die pad. In accordance with FIG. 12, the sheet 110 is made of pure silver plate of 20 μm thick, and the grooves 111 of 10 μm deep are formed on

one side of the sheet. The grooves are formed by press manufacturing or half cut manufacturing with a dicing plate. The Ag sheet is annealed after roll manufacturing and grooves manufacturing so that the hardness of the Ag sheet becomes equal to or less than 35 Hv.

In accordance with using the Ag sheet of the present embodiment for performing the thermosonic thermocompression bonding of chip/die pad, the composition deformation of the Ag sheet is readily proceeded by the presence of the grooves and softness of the material, and tight and high heat resistant bonding can be achieved without damaging the chip, because newly generated planes are formed and the bonding process is proceeded readily at the boundary of the bonding planes under the condition that the stress added to the Si chip is small. And, a semiconductor package having high temperature cycle reliability can be provided, because the thermal strain between the chip/die pad accompanied with heat generation of the chip during use of the package can be absorbed by the soft Ag sheet having the groove space.

FIG. 13 indicates one of other embodiments of the bonding sheet for bonding the chip and the die pad. In accordance with FIG. 13, the core portion 112 of the bonding sheet is the Ag sheet manufactured as same as the Ag sheet indicated in FIG. 12. The surface of the Ag sheet is plated with Sn 113 of 0.3 - 2.0 μm thick.

In accordance with using the bonding sheet of the present embodiment for performing the thermosonic

thermocompression bonding of chip/die pad, a liquid phase is formed at a heat temperature of above 220 ℃ by a Ag-Sn reaction, and the surface of the sheet is covered with thin film of the liquid. Therefore, such an advantage is realized that ensured and tight bonding can be achieved readily under a low compressing condition, because the liquid in the region where the sheet is compressed to the die pad or chip rear plane electrode is ejected outside and the bonding between the members having a high melting point each other is proceeded readily. Furthermore, because Ag is supplied by dissolving or diffusion during heating from the core to the Ag-Sn layer ejected from the bonding interfaces , the melting point of the Ag-Sn layer is elevated finally higher than 470 ℃, and the bonding portion can have high heat resistance. Regarding reliability as the semiconductor package, the same advantages as the embodiment indicated in FIG. 1 can be obtained.

FIG. 14 indicates one of other embodiments of the bonding sheet for bonding the chip and the die pad. In accordance with FIG. 14, the bonding sheet is a mesh shaped sheet composed of Ag wires 114, 115 woven in vertical and horizontal directions.

In accordance with the present embodiment, the bonding sheet has bumps and dips such as the thickness at the portion where the Ag wires are overlapped is thick and the thickness at the other portion is thin. Therefore, the composition deformation at the thick portion can be

proceeded readily, and the same advantages as the embodiment indicated in FIG. 12 can be obtained.

FIG. 15 indicates an embodiment of the semiconductor package of the present invention, wherein Ag particles are used for bonding the chip and the die pad. In accordance with FIG. 15, the Al electrode 121 is formed on the circuit forming plane of the semiconductor chip 120, and plural Ag bumps 125are formed thereon. On the rear plane of the chip, the rear plane electrode 122, outermost surface of which is plated with Ag, is formed. The lead 123, which is plated with precious metal , on the circuit forming plane and the Ag bumps are directly bonded by thermosonic thermocompression bonding. The chip rear plane electrode and the die pad terminal 124, which is plated with precious metal , are bonded by thermosonic thermocompression bonding interposing the Ag particles 126, which are composed of mixing with the resin 127 in a ratio of more than 90 % by volume Ag. The amount of the resin is determined so small that the resin pushed out during the compression is not flown down from the side plane of the die pad terminal onto the compression stage, and so much that the mixture can be treated as a viscous liquid. The resin is thermosetting resin, and the resin is cured by heating at the bonding. The Ag particles and the Ag deposition film at the rear plane of the chip, the Ag particles and the die pad terminal, and the Ag particles themselves are bonded partly by metal bonding in the region of contacting portions. The size of the die pad terminal

is as much as capable of being contained into the resin body 128, and as same as the size of the chip. It may be somewhat larger or smaller than the chip.

In accordance with the present embodiment, a small and thin semiconductor package having a low electrical resistance, and containing no Pb can be provided. Because the Ag particles are mixed with resin, dispersion of the Ag particles can be prevented by the viscous property of the resin, and productivity can be improved by readiness of the Ag particle supply to the bonding portion. Because narrow gaps between the Ag particles after bonding can be filled with the mixed resin, the necessity to filled the gaps with the molding resin can be eliminated, and such an advantage is realized that the generation of voids can be decreased significantly and the production yield can be increased. Furthermore, although the bonding agent is a mixture of the resin and Ag particles, the thermo-compressing bonding method using concurrently ultrasonic vibration is used for the bonding. Therefore, the resin is pushed out from the bonding interface of the metals , and a tight bonding of metals each other is achieved at the bonding portion. Accordingly, an advantage that the bonding reliability is remarkably improved in comparison with the adhesion with the Ag paste can be realized.

FIG. 16 indicates an embodiment of the semiconductor package of the present invention, wherein a Ag sheet having grooves is used for bonding the chip and the die pad. In accordance with FIG. 16, the Au balls 139 are formed on

the Al electrode 131 of the chip 130, and Ag deposition film is formed on the outermost surface of the rear plane electrode 132. Surface of the lead terminal 135 and the die pad terminal 138 are plated with Pd. The Ag sheet 140, whereon the grooves 141 are formed, is inserted between the rear plane of the chip and the die pad terminal. Respective of the bonding portions is directly bonded by thermo-compression bonding method concurrently using ultrasonic vibration. The lead terminals are protruded from a side plane of the resin body, and manufactured to be folded.

In accordance with the present embodiment, in addition to the same advantages as the embodiment indicated in FIG. 2, breakage of the respective bonding portions of Al electrode/Au ball/lead terminal by thermal strain and the like can be decreased, and reliability of the semiconductor package can be improved, because the resin bonding area at the upper and lower regions of the lead terminals can be taken wide as the lead terminals are protruded from only one side, and a compression force between the lead/chip by the force of curing shrinkage of the resin can be increased.

FIG. 17 indicates an embodiment of the semiconductor package of the present invention, wherein a part of the lead terminal is exposed at upper plane of the resin body. In accordance with FIG. 17, the Au balls 154 are formed on the Al electrode 146 of the chip 145, and Ag deposition film is formed on the outermost surface of the rear plane

electrode 147. Surface of the lead terminal 150 and the die pad terminal 153 are plated with Pt/Au 149, 152. The Ag sheet 155, whereon the grooves 156 are formed, is inserted between the rear plane of the chip and the die pad terminal. Respective of the bonding portions is directly bonded by thermo-compression bonding method concurrently using ultrasonic vibration. The lead terminals are protruded from a side plane of the resin body and manufactured to be folded, and the lead terminal is exposed at upper surface of the resin body.

In accordance with the present embodiment, in addition to the same advantages as the embodiment indicated in FIG. 2, heat resistance of the semiconductor package can be decreased significantly, because the heat can be released effectively from the wide area of the lead terminal exposed at upper surface of the resin body.

FIG. 18 indicates an embodiment of the wiring substrate for mounting the semiconductor package of the present invention. In accordance with FIG. 18, the wiring substrate 160 is a multi-layered organic substrate composed by laminating substrates, which are composed by forming Cu foil pattern on a epoxy-glass cloth composite. Various semiconductor packages and connection terminals 165, 169, 170, 171 of passive devices are formed on the surface of the substrate. The connection terminals for mounting the semiconductor of the present invention is composed of the connection terminals 161, 168 for drain, the connection terminals 164, 167 for source, and the

connection terminals 162, 163, 166 for gate, all of which are in a size that is containable in the body of the package. FIG. 19 indicates an embodiment of an electronic device, wherein the wiring substrate indicated in FIG. 18 is mounted with the semiconductor packages of the present invention, LST packages, and elements. In accordance with FIG. 19, the LSI packages 176, 177, 178 for signal processing, the vertical semiconductor packages 172, 175, and resistance and passive device of capacitance 173, 174 are mounted on the wiring substrate by soldering connection.

In accordance with the present embodiment, the connecting area between the power semiconductor package and the substrate can be taken wide, and the chip, i.e. a heater, and the substrate can be connected with the shortest distance. Therefore, temperature difference between the substrate and the package can be decreased, the stress generated at the solder connecting portions can be decreased, and a highly reliable electronic device can be provided. Because heat generation of the package is decreased, the temperature of the device is not elevated beyond the normal operating temperature range, even though any special heat releasing device is not provided. Accordingly, such advantages are realized that the structure of the electronic device can be simplified, cost is suppressed, and life of the electronic device can be improved due to the low temperature rise during operation.

As explained in detail above, in accordance with the present invention, the electrical resistance of the package can be decreased.

FIG. 29 indicates changes of strength at bonding portions, when Au ball bonding is performed on Al electrode film of 3.5 μm thick at 200 ℃ of bonding temperature, and the bonding portions are held at a high temperature. When the holding temperature is lower than 200 ℃, decrease of the strength can be observed in a short time, but the higher the holding temperature is, the sooner the strength is increased again. And the holding time is further extended, the strength is decreased again. As the result of analyzing the reason of the above phenomenon in detail, it was revealed that the strength immediately after the bonding depends on the strength of Al film itself; the first decrease of the strength at the initial stage of holding at the high temperature is caused by growing an $AuAl_2$ compound, which is known conventionally and called as purple plague, at the boundary of a AuAl alloy layer and the Al film. Furthermore it was revealed that the increase in strength is caused by changing all the Al film at the bonding portion to the AuAl alloy layer, which is stronger than Al, and subsequent decrease in the strength is caused by growing defects called as carkendahl voids at the boundary plane of the Au/AuAl alloy layer. It was found that the increase in the strength as much as twice of the bonding strength is caused by the presence of fine bumps and dips on the surface of the transistor chip

corresponding to a large number of cell structure, and the alloy layer and the Si substrate forms a mechanical meshing structure. This is a phenomenon, which does not occur with conventional LSI devices. It was found that, after performing a heat treatment for a short time at a high temperature higher than 250 ℃, grow of the carkendahl voids did not become any problem at a heating temperature of 150 ℃ and the holding time of 2000 hours, and the decrease in the strength was not generated as indicated in FIG. 30. The inventor of the present invention utilizes the above phenomenon and achieved the improvement of the initial bonding strength as much as approximately twice, and the improvement of the reliability for connection at the metallic bonding portions themselves during the temperature cycle in the region lower than 150 ℃, i.e. the temperature for practical use, and holding at a high temperature. Furthermore, regard to the bonding the lead for electrode with the Au bumps on the chip, an thermosonic thermocompression bonding method, which is performed under a low temperature (lower than 250 ℃) and a low load without damaging the chip, has been developed, which makes it possible to bond at a low temperature. Accordingly, in view from the above, thermal strain generated during the cooling step in the bonding operation could be decreased significantly, and the reliability of the connection at the metal bonding portions could be improved. Simultaneously, in accordance with realization of the low temperature bonding method, it

becomes possible to perform the metallic bonding and the resin adhesion simultaneously by filling the resin into the gap between the electrode lead/chip when bonding the electrode lead/ chip. Then, because the resin is pushed out by compression, resin can be filled with no void, and because the bonding can be achieved in a condition that compression force is added to the Au bumps by curing shrinking phenomenon of the resin, fatigue life can be extended by the effect of the compression stress, even if temperature cycle is added.

Next, high reliability of package, which does not contain Pb and is omitted with resin sealing, is explained hereinafter. The transistor package is composed of a structure, wherein three independent metallic components are connected electrically with respective electrode of the chip and fixed in the structure. Conventionally, the fixing the respective metallic components have been performed with cured resin. However, in accordance with the structure of the present invention, the metallic components are fixed by bonding the respective component with the chip flexibly and tightly by concurrent use of metallic bonding and resin adhering. The reason to use the metallic bonding and the resin adhering concurrently is that, although a high strength can be achieved by only the metallic bonding, but if the cu, which is a core material of the metallic component, is bonded with Si chip tightly, a large strain is generated in the Si chip by difference of thermal expansion of the Cu and

the Si chip, and deterioration of their characteristics, or in an extreme case, damage of the chip can be generated. Therefore, it is necessary to make the bonding portion have the flexible structure for absorbing the strain, and as the metallic bonding structure having spaces, the structure of the present invention, wherein insufficient bonding strength is reinforced by resin adhesion, is realized. In accordance with the structure of the present invention, if the resin is used in a shape of film, the resin adhering and the metallic bonding can be performed in a same bonding step, simultaneously, mold-bake step of the resin can be omitted. Accordingly, production cost can be decreased, the productivity can be improved, and the transistor package, which is desirable in view of environmental problem, can be provided. In accordance with performing the metallic bonding by thermosonic thermocompression method; treating the surface of the metal with spatter cleaning before bonding; and changing the bonding force from low loading to high loading in a slope shape under adding the ultrasonic waves; metallic bonding having a high strength under the condition that the deformation of the bumps is small can be achieved.

Hereinafter, embodiments of the present invention are explained in detail referring to drawings.

Fig. 22 indicates an embodiment of the structure of the transistor package relating to the present invention. In accordance with FIG. 22, the Al electrode 2 of 2 μm thick is formed on the circuit forming plane of the

transistor chip 1, and the rear plane electrode 3, outermost surface of which is plated with Au, is formed on the opposite plane of the transistor chip 1. The Au bumps 7 are formed on the Al electrode by ball bonding method. In this step, all the Al electrode film under the bumps is changed to a AuAl alloy 9 by heat treatment of, for instance, 300 ℃ - 2 hours, or 250 ℃ - 10 hours. Surface of the metallic lead 4 is plated with Pd/Au, and the metallic leads are bonded with the Au bumps formed on the Al electrode by incorporated thermosonic thermocompression bonding method at a relatively low temperature such as lower than 250 ℃. The first resin 8 is supplied in a shape of sheet at the thermosonic thermocompression bonding, and adhered and cured simultaneously with the bonding of the Au bumps. The height of the bumps (resin thickness) after bonding is several tens microns. The chip rear plane electrode and the die pad mounting lead 6 hold the second resin 11 sheet, wherein precious metal particles are buried, between them, and the chip rear plane electrode and the die pad mounting lead 6 are bonded by compression with adding ultrasonic waves and heating at a relatively low temperature such as lower than 250 ℃. The precious metal particles, i.e. Ag particles 10 in this case, are deformed by compressing to the rear electrode and the die pad, and made a metallic bonded condition. The die pad mounting leads are manufactured previously to be folded, and the bonding condition is controlled so that the lower plane after

deforming and bonding the Ag particles is approximately in a same plane as the plane of the electrode lead. The first and second resin are adhered with the upper and the lower members, and give a compression stress to the bonding portion by the shrinking phenomenon at the curing time. Here, thermo-adhering polyimide resin is used as the first and second resin, but epoxy resin, which can be cured at room temperature, and other resin may be used.

In accordance with the present embodiment, the strength at the bonding portions of Al electrode/Au bump/electrode lead can be increased by making all the Al under the bonding portions of the transistor package an alloy, decrease of the strength by holding the bonding portions at a high temperature is prevented, and a structure, wherein the compression force is applied to the bonding portions by the effect of the resin adhering, is composed. Accordingly, a highly reliable and low resistant transistor package having a significantly extended temperature cycle life can be provided. Because the bonding temperature in the compression bonding of the metals each other is lowered as lower than 250 ℃, concurrent bonding with the resin adhering becomes possible, and filling and adhering the resin with no voids also becomes possible. Furthermore, the residual stress at the bonding portions can be decreased by lower temperature bonding. Accordingly, in view of the above points, the reliability of the transistor can be improved.

In accordance with the bonding structure, wherein

the rear plane electrode of the chip and the die pad mounting leads are bonded by concurrent use of the metallic bonding and the resin adhering, of the present embodiment, and thermal and electrical conductivity at the bonding portions are ensured, and simultaneously, the difference in thermal expansion between the chip and the die pad mounting leads are absorbed by the deformation of the space filled with the resin. Furthermore, the temperature cycle life of the die pad-bonding portions can be improved by compression load applying effect to the metallic bonding portion accompanied with the curing shrinkage of the resin, and the package containing no Pb, having concurrently desirable electrical and thermal conductivity, temperature cycle reliability, and solder reflow endurance can be provided.

Furthermore, in accordance with the above two reasons, the reliability of the package can be ensured without performing the resin sealing. Accordingly, a small size and low resistant transistor package; which can save resin, decrease the production cost and the production tact by omitting the molding step, and is desirable in view of environmental problem; can be provided.

Because the bonding portions of the Al electrode and the Au bumps are changed to a Au-Al alloy for strengthening by heat treatment in the step to bond the chip with the electrode lead via Au bumps by the thermosonic thermocompression bonding method, even if the Au bumps are ruptured by adding a load and vibration from the chip side

or the lead side for compression bonding, the Si substrate or the transistor element under the bumps is not damaged such as generation of cracks. Accordingly, generation of failed products by the bonding damage can be prevented, and production yield can be improved.

FIG. 23 indicates one of other embodiments of the structure of the transistor package relating to the present invention. In accordance with FIG. 23, the Al electrode 16 of 5 μm thick are formed on the circuit forming plane of the transistor chip 15, and the rear plane electrode 17, outermost surface of which is made of Ag, is formed on the opposite plane. The Au bumps 20 are formed on the Al electrode by ball bonding method. In this step, all the Al electrode film under the bumps is changed to a Au-Al alloy layer 21 by heat treatment of, for instance, 300 ℃ - 2 hours, or 250 ℃ - 10 hours. The openings 25, 26 are formed in the chip facing regions of the electrode lead 16 and the die pad mounting lead 19, and all the surface of the members is plated with Pd/Au flush plating. The electrode lead is bonded with the Au bumps formed on the Al electrode by incorporated thermosonic thermocompression bonding method at a relatively low temperature as lower than 200 ℃. The first resin 22 is supplied in a form of sheet, and adhered and cured simultaneously with the bonding of the Au bumps. The height of the Au bumps (resin height) is several tens microns. The chip rear plane electrode and the die pad mounting leads hold the second resin 24 in a shape of sheet, wherein

precious metal particles are buried, between them, and the chip rear plane electrode and the die pad mounting lead are bonded by compression with adding ultrasonic waves and heating at a relatively low temperature as lower than 250 ℃. The precious metal particles, i.e. the particles made of Ag in this case, are deformed by compressing to the rear electrode and the die pad mounting lead with heating, compressing, and ultrasonic vibrating, and made a metallic bonded condition. The first and second resin are adhered with the upper and the lower members, and give a compression stress to the bonding portion by the shrinking phenomenon at the curing time.

In accordance with the present embodiment, the package of high reliability, low resistance, and desirable in view of environment problem can be provided as well as the package indicated in FIG. 22. Furthermore, because the electrode and the resin, and the die pad mounting lead and the resin are bonded tightly by the mechanical bonding at the openings, in addition to the chemical bonding (adhering) at the boundary plane, peeling off the resin adhered portions is not generated even under a high temperature and high humidity environment and the temperature cycle environment, the strain added to the metallic bonding portions of the Au bumps and Ag particle can be decreased, and reliability of the package can be improved significantly.

FIG. 24 indicates one of other embodiments of the structure of the transistor package relating to the present

invention. In accordance with FIG. 24, the Al electrode 31, 32 of 3.5 μm thick are formed on the circuit forming plane of the transistor chip 30, and the rear plane electrode 33, outermost surface of which is Ag, is formed on the opposite plane. The Au bumps 43 are formed on the Al electrode by ball bonding method. All the surface of the members of the electrode leads 36, 39 and the die pad mounting lead 42 are plated by Pd/Au flush plating 35, 38, 41. The electrode leads and the Au bumps formed on the Al electrode are bonded by the incorporated thermosonic thermocompression bonding method at relatively low temperature as lower than 200 ℃. The first resin 44 is supplied in a liquid state to fill into gaps after the thermosonic thermocompression bonding, and adhered and cured. The chip rear plane electrode and the die pad mounting leads hold the second resin 48 in a shape of sheet, wherein precious metal particles are buried, between them, and the chip rear plane electrode and the die pad mounting lead 42 are bonded by compression with adding ultrasonic waves and heating at a relatively low temperature as lower than 250 ℃. The precious metal particles 47, i.e. the particles made of Cu 45 of 30 μm, the surface of which is plated with Ag 46 by 5 μm thick in this case, are deformed by compressing to the rear electrode and the die pad mounting lead with heating, pressing, and ultrasonic vibrating, and made a metallic bonded condition. The first and second resin are adhered with the upper and the lower members, and give a compression stress to the bonding

portion by the shrinking phenomenon at the curing time. The two electrode leads and the die pad mounting lead are arranged at opposite planes respectively interposing the chip between, and the size of the respective lead is approximately as same as the size of the chip.

In accordance with the present embodiment, the package of high reliability, low resistance, and desirable in view of environment problem can be provided as well as the package indicated in FIG. 22. Furthermore, because Ag plated Cu particles having cores made of Cu, which is cheaper than precious metal s, are used for bonding the chip rear plane electrode with the die pad mounting lead, the component cost can be decreased. Further, because the planes of the external connection terminals are arranged at upper and lower sides of the chip, a structure, wherein the mounting can be performed by holding the package from both sides of the chip, can be adopted, and the mounting by mechanical contact can be performed readily. The chip size package can be realized, and high density mounting becomes possible by decreasing the mounting area.

FIG. 25 indicates one of other embodiments of the structure of the transistor package relating to the present invention. In accordance with FIG. 25, the Al electrode 51 of 3.5 μm thick is formed on the circuit forming plane of the transistor chip 50, and the rear plane electrode 52, outermost surface of which is plated with Au, is formed on the surface of the opposite plane. The Au bumps 61 are formed on the Al electrode by ball bonding method. In

this step, all the Al electrode film under the bumps is changed to a Au-Al alloy layer 62 by heat treatment of, for instance, 300 ℃ - 2 hours, or 250 ℃ - 10 hours. Surface of the electrode lead 55 is plated with Pd/Au 54, and the electrode leads are bonded with the Au bumps formed on the Al electrode by incorporated thermosonic thermocompression bonding method at a relatively low temperature as lower than 200 ℃. The chip rear plane electrode and the die pad leads hold the die pad bonding resin 60 in a shape of sheet, wherein precious metal particles 59 are buried, between them, and the chip rear plane electrode and the die pad lead 42 are bonded by compression with adding ultrasonic waves and heating at a relatively low temperature as lower than 250 ℃. The precious metal particles 47, i.e. the particles made of Ag in this case, are deformed by compressing to the rear electrode and the die pad mounting lead with heating, pressing, and ultrasonic vibrating, and made a metallic bonded condition. Whole of the chip and the respective leads are covered with mold resin except the external connection terminals. A compression stress is given to the bonding portions of the chip and respective of the leads by the shrinking phenomenon of the resin at the curing time.

In accordance with the present embodiment, the bonding portion of the Au bumps with the Al electrode film is strengthened as twice as the normal strength by alloying to the Au-Al alloy, and the $AuAl_2$ compound having weak strength, which is generally formed by holding the package

at a high temperature, is not formed. Therefore, the low resistant transistor package having superior temperature cycle reliability can be realized.

FIG. 26 indicates an embodiment of the die pad-bonding adhering film of the present invention.

In accordance with FIG. 26, the precious metal particles 66 are buried into the resin film 65 in a condition that a part of the particle is exposed to the surface of the resin film. The precious metal particle is selected from the group consisting of respective particle of Ag, Au, Pd, Pt, and particles obtained by plating respective of Cu, Ni cores with Ag, Au, Pd, and Pt, respectively. The sizes of the particles are composed that a large number of the particles having at least a half of the film thickness are contained therein. The resin film is selected from the group consisting of polyimide resin, epoxy resin, polyester resin, and phenol resin, and the resin is manufactured to a condition that thermoplastic and thermosetting properties are concurrently provided (a condition that the solvent is evaporated and the resin is semi-cured).

FIG. 27 indicates one of other embodiments of the die pad-bonding adhering film of the present invention.

In accordance with FIG. 27, the precious metal particles 68, 69 are exposed to both surfaces of the resin film 67.

FIG. 28 indicates a method for adhering two members using the die pad-bonding film indicated in FIG. 26. In

the step (A) in FIG. 28, the chip member 70, whereon a precious metal thin film is deposited, the die pad-bonding film 71, wherein Ag particles 72 are buried, and the die pad mounting lead 73, the bonding plane of which is plated with thick Ag, are laminated and positioned. Then, in the step (B) of FIG. 28, the laminated work is placed on the heating stage 74, and compressed by adding the load 73 with the bonding tool 76 via the organic film 77. At the time when the temperature of the work is elevated to a designated degrees, ultrasonic vibration 79 is added to the bonding tool in order to push in the chip member into the die pad-bonding film with rupturing the Ag particles for metallic bonding the chip member with the die pad mounting lead via the Ag particles, and adhering the chip member and the die pad mounting lead by the die pad-bonding film. The temperature at the start of adding the ultrasonic waves is the temperature at which softening the die pad-bonding film begins, and the final heating temperature is the temperature at which the die pad-bonding film is cured. The organic film interposed between the bonding tool and the chip member is changed every operation or per several operations. Accordingly, such a method is adopted that the organic film is supplied in a rolled tape state, and transferred orderly to the operating portion for changing. The material of the organic film is composed of an organic material having a high glass transition temperature, which does not become soft at the bonding temperature. The condition after bonding is indicated in

(c) of FIG. 28. The chip member and the die pad mounting lead are bonded metallically at plural portions via one or two of Ag particles, and an excess amount of the die pad-bonding film is pushed outside from the gap between the both members. Accordingly, no void is generated in the resin filling the gap.

In accordance with the present embodiment, a clean metallic surface of the Ag particle can be compressed onto the chip member, because the Ag particles are exposed out from the die pad-bonding film; the Ag particle can be deformed certainly, and microscopic plastic flow of the both metallic members is made to be generated, because the size of the Ag particle is made larger than the gap; and the ensured metallic bonding becomes possible by adding the ultrasonic vibration. On the other hand, in accordance with the bonding step of the Ag particles with the die pad mounting lead, the Ag particle contacts with the die pad mounting lead by pushing away the resin film, which is softened by elevation of the temperature, in the step that laminated work is placed on the heating stage and the load is added by the bonding tool via the chip. At this time, the resin is still in a solid state and does not make the surface of the metal wet, and the Ag particle and the die pad mounting lead can be contacted each other with clean metallic boundary. Therefore, ensured metallic bonding becomes possible by adding the ultrasonic vibration. The resin becomes once a liquid state by heating after tight contact of the Ag particles and the

die pad mounting lead. After the excess amount of the resin is pushed outside through the gap between the chip and the die pad mounting lead, its curing starts. In accordance with the phenomenon described above, the two members are certainly bonded metallically via the Ag particles, and simultaneously, the adhering with the resin is proceeded concurrently. Therefore, the number of the bonding steps can be decreased, and improvement of productivity can be realized.

Because the organic film is inserted between the bonding tool and the chip member as a consumable article, damages of the chip member by contacting with the hard bonding tool can be prevented, and the production yield of the package can be increased. Furthermore, consumption of the bonding tool can be prevented, and usable cycles of the apparatus can be increased significantly. Accordingly, decrease of the production cost can be realized.

As described above in detail, in accordance with the present invention, the semiconductor package, wherein the strength of the bonding portions of Al electrode/Au bumps/ electrode lead is increased, can be provided.

FIG. 31 indicates an embodiment of the present invention in a case when the bump containing precious metal at front plane side electrode is made an alloy with low melting point metals.

In accordance with FIG. 31, the metalized film 289 of Ti/Ni/Au, Ti/Ni/Ag, Cr/Cu/Ni/Au, or Cr/Cu/Ni/Ag, in a

specified pattern is formed on the front plane side Al electrode pad 282 of the vertical semiconductor element 281, and the metalized electrode 283, outermost surface of which is Ag or Au, is formed on the rear side plane. The die pad 286 is connected metallically with all over the surface of the metalized electrode 283 by the solder 287 containing Ag-Sn as a basic composition, for instance, Ag-Sn-Pb, Ag-Sn-Pb-Cu, and the like. The lead 284 is connected metallically with the front plane side metalized film 289 by the alloy bumps 285 containing Ag-Sn as a basic composition. The connecting portion is formed only in a specified region, wherein the metalized film 289 of the front plane side electrode is formed. The semiconductor element, the lead, and a part of the die pad is protected by covering with resin 288. The lower plane of the die pad is exposed to the surface of the resin body, and reshaped in a condition that the die pad is protruded out horizontally from the plane of the resin body opposite to the lead. The lead is protruded from the middle portion of the side plane of the resin body, and folded so that the lower plane of the lead is reshaped to be approximately same level as the lower plane of the die pad. Here, the approximately same means a range that the difference in height is within the thickness of the lead or the die pad.

FIG. 32 indicates an embodiment of the present invention in a case when the semiconductor package indicated in FIG. 31 is mounted on a wiring substrate.

In accordance with FIG. 32, Ni/Au film is formed

on the surface of the connecting terminals 291, 293 formed on the wiring substrate 290, and the lead 284 of the package is connected to the lower plane of the die pad 286 with a low melting point metal, which is capable to connect at an operating temperature lower than the melting point of the connecting alloy 285, 287 in the package. When the connecting alloy in the package is Ag-Sn-Cu group, the wiring substrate connecting alloy is a solder of Sn-Bi group or Sn-In group. When the connecting alloy in the package is Ag-Sn-Pb group, a solder of Sn-Ag group is used as the wiring substrate connecting alloy.

In accordance with the present embodiment, the chip electrode and the lead are connected by the bumps. Accordingly, because the connection distance is short and the connecting area, that is, conducting area is wide, the electrical resistance at the connecting portion can be decreased. In accordance with forming the bumps with an alloy composed of precious metal added with low melting point metals, the using amount of the precious metal can be decreased, and the surface of the leads can be composed with the low melting point metals. Accordingly, the cost for the members can be decreased. On the contrary, when the surface electrode is connected with a fused alloy, a short circuit between the adjacent two electrodes becomes a problem. However, in accordance with the present embodiment, the metalized film, which is wettable with the connecting alloy formed on the chip side electrode, is restricted to form in a specified region. Accordingly,

even if the distance between the electrodes are short, the short circuit accident can be prevented, because the fused metal is not spread widely, nor come to close. In accordance with the present embodiment, the chip electrode is connected to the upper and lower metallic members with the fused metal, any external force is not added to the chip electrode during the connection operation. Therefore, the assembling yield can be increased by preventing damage of the chip, and the cost for production can be decreased. On account of protruding the pad from the side plane of the resin body horizontally, the soldering portion for mounting onto the wiring substrate can be seen by eyes, and soldering failure can be inspected readily and generation of defective product can be prevented previously.

In accordance with the present embodiment, the low melting point alloy containing precious metal is used as the material for the bumps, but a low melting point alloy containing no precious metal has the same advantages as the present embodiment.

FIG. 33 indicates an embodiment of the present invention in a case when the semiconductor package by the present invention, die pad of which is omitted, is mounted on the wiring substrate.

In accordance with FIG. 33, the Au bumps 257 are formed on the front plane side Al electrode pad 252 of the vertical type semiconductor chip 251, the bumps are connected metallically to the lead 256 plated with precious

metal , and periphery of the bumps are reinforced by the first 261. The metalized electrode 253 at the rear plane of the chip is connected directly to the connection pad 259 of the wiring substrate 258 with the solder 260. The external connecting plane of the lead is connected to the connecting terminals with the same kind of solder. The metalized electrode plane at the rear plane of the chip and the external connecting plane of the lead are formed so that their height become approximately same level each other, in other words, the difference of the height is within the thickness of the lead. In accordance with FIG. 33, the lead and the chip are exposed outside in the condition mounted onto the substrate. However, if the environment is not desirable, the lead and the chip may be covered with the second resin by potting.

In accordance with the present embodiment, the die pad is not used, and the package structure becomes simple. Therefore, the cost for assembling and the cost for the components can be decreased, and the production cost can be decreased significantly. Because the electrode at the rear plane of the chip is connected directly to the connecting terminals of the wiring substrate by soldering, the electrical resistance between them can be decreased, and an on-resistance of the package can be decreased. The height of the package can be decreased as much as the die pad omitted, an ultra thin substrate mounting can be realized. If the package is sealed with a potting resin after mounting, the temperature cycle reliability at the

connecting portion at the rear plane of the chip is improved in comparison with the conventional structure using the die pad, and an electronic apparatus having high reliability can be realized.

FIG. 34 indicates an embodiment of the present invention in a case when the plane mounting type semiconductor package by the present invention is mounted on the wiring substrate.

In accordance with FIG. 34, the Au bumps 268 are formed on the Al electrode pad of the vertical type semiconductor chip 262, the bumps are connected metallically to the lead 267, surface of which is plated with precious metal . A metalized layer, outermost surface of which is precious metal , is formed at the rear plane of the chip, and the metalized layer is connected electrically to the die pad 269 plated with precious metal with precious metal particles 271. The chip, the lead, and a part of the die pad are covered with the resin 272 for protection and reinforcement. The lower plane of the die pad is exposed to the bottom surface of the resin body and protruded to the side plane. On the other hand, the lead is protruded from the middle portion of the opposite side plane of the resin body, manufactured to be folded so that the height of the external connecting portion becomes approximately as same as the height of the external connecting portion of the die pad. The plane mounting is performed by connecting to the connecting terminals of the wiring substrate by soldering. Because the connecting

terminals are aligned approximately at a definite height in the range of several tens microns, the external connecting terminals of the package must be aligned with their height. In accordance with the present embodiment, small variation in height can be absorbed by the difference of the thickness of the solder 275, and allowable difference of the height (ΔH) is as same as the difference in the thickness of the lead (smaller than approximately several hundreds micron). The plane mounting package may be any package, if the difference of the external connecting plane facing to the wiring substrate of which is controlled within the thickness of the lead or the die pad.

In accordance with the present embodiment, a structure, wherein the die pad is protruded from the side plane of the resin body, is adopted. Accordingly, the solder connecting portion can be confirmed by eyes from up side when the package is mounted onto the wiring substrate, and connecting portions can be inspected readily, and production velocity is increased. Furthermore, the cost for assembling can be decreased, and operability is improved.

FIG. 35 indicates a plan view of the vertical semiconductor element used in assembling the semiconductor package by the present invention, and an example of its cross sectional structure.

In accordance with FIG. 35, n-type epitaxial layer 315 is formed on the high concentration n-type substrate

314, and p-type and n-type patterns are formed in the layer in a condition that depths and shapes are controlled. The gate oxide film 316 is formed at a position, where includes the p-type diffusion layer 316 formed so as to surround the contact area of the source electrode, and n-type layers 317, 318, at right and left. The gate electrode line 320 is formed on the oxide film. The gate electrode line is coated with the insulating layer 321 so as not to contact with the source electrode pad 312, and connected to the gate electrode pad 313. Generally, aluminum is used as the material of the gate and source electrode pad, but some cases, other metal is metalized thereon. Generally, the plane whereon the pattern of the diffusion layer is formed is called as the front plane, and the opposite plane is called as the rear plane. The present element is so-called MOSFET, which controls the current passing through source/drain in accordance with the presence of, or magnitude of the voltage added to the gate electrode. Decrease of the on-resistance of the present element is remarkably advantageous in view of power loss. An effect to decrease the resistance is achieved by controlling the profile of the npn structure in the epitaxial layer and impurity concentration, but most effective method is to shorten the conducting distance by decreasing the thickness of the wafer. Therefore, pn elements, circuit patterns, and electrode pads are formed on the surface of Si wafer, the thickness of which makes it possible to handle the wafer in the

manufacturing steps. Subsequently, the rear plane of the wafer is ground to make the high density n-type substrate 314 thin, and finally, the drain electrode metalized layer at the rear plane is formed to produce the element.

In a case when the rear plane ground element of the present embodiment is used, the contacting area with the metalized layer is increased, because the grinding mark at the rear plane forms adequate bumps and dips, and the bumps and dips perform further a role of an anchor effect. Therefore, because ohmic contact resistance of the rear plane electrode is decreased, and adherence of the rear plane electrode with the metalized layer is increased, the improving effects in both electrical characteristics and reliability can be realized.

The present invention is applicable to not only MOSFET, but to all the element, resistance or impedance of which must be decreased, such as diodes, thyristors, photo-elements, and the like.

What is claimed is:

1. A semiconductor device comprising:

a semiconductor substrate,

a semiconductor element which comprises;

a first electrode provided on front plane of said semiconductor substrate, and a second electrode provided on rear plane of said semiconductor substrate,

a first metallic member connected to said first electrode, and

a second metallic member connected to said second electrode, wherein:

said first electrode is connected to said first metallic member via a first metallic body including a first precious metal, and

said second electrode is connected to said second metallic member via a second metallic body including a second precious metal .

2. A semiconductor device as claimed in claim 1, wherein:

a surface portion of said first metallic member for connecting with external line and a surface portion of said second metallic member are positioned at substantially a same level.

3. A semiconductor device as claimed in any of claims 1 and 2, wherein:

said first metallic body is a projecting convex electrode terminal protruded from any of said first electrode and said first metallic member.

4. A semiconductor device as claimed in any of claims 1 and 2, wherein:

said first metallic body is plural projecting convex electrode terminals protruded from any of said first electrode and said first metallic member, and

said plural projecting convex electrode terminals are distributed on substantially whole bonding interface between said first electrode and said first metallic member with substantially same intervals.

5. A semiconductor device as claimed in any one of claims from 1 to 4, wherein:

a precious metal layer is provided on bonding surface of said first metallic member.

6. A semiconductor device as claimed in any of claims 1 and 2, wherein:

said second metallic body is a metallic layer positioned at the bonding interface between said second electrode and said second metallic member.

7. A semiconductor device as claimed in claim 6, wherein:

said metallic layer is composed by bonding each other

a precious metal layer positioned at the bonding front plane of said second electrode with a precious metal layer positioned at the bonding front plane of said second metallic member.

8. A semiconductor device as claimed in claim 6, wherein:

said metallic layer is an alloy layer having a solidus line temperature at least 400 ℃, which contains a precious metal as a main component.

9. A semiconductor device as claimed in claim 1, wherein:

said first metallic member comprises plural portions extended from a portion having a bonding portion with said first electrode, and

respective of said plural portions comprises a surface portion for connecting with an external line.

10. A semiconductor device as claimed in claim 3, further comprising:

an insulator for covering said semiconductor element and said first and second metallic members, wherein:

the plane of said first metallic member at rear of the plane bonded with said first electrode comprises an exposed portion for connecting with an external line.

11. A semiconductor device as claimed in claim 10, wherein:

said bonded plane of said semiconductor element is a circuit forming plane, and said first electrode is a main current electrode.

12. A semiconductor device as claimed in claim 6, further comprising:

an insulator for covering said semiconductor element and said first and second metallic members, wherein:

the plane of said second metallic member at rear of the plane bonded with said second electrode comprises an exposed portion for connecting with an external line.

13. A semiconductor device comprising:

a semiconductor substrate,

a semiconductor element which comprises;

a first electrode provided on front plane of said semiconductor substrate, and a second electrode provided on rear plane of said semiconductor substrate,

a first metallic member connected to said first electrode, and

a second metallic member connected to said second electrode, wherein:

said second electrode is connected to said second metallic member via a metallic layer containing precious metal , and

said metallic layer is composed by bonding each other a precious metal layer provided at the bonding front plane of said second electrode with a precious metal layer provided at the bonding front plane of said second metallic member.

14. A semiconductor device comprising:

a semiconductor substrate,

a semiconductor element which comprises;

a first electrode provided on front plane of said semiconductor substrate, and a second electrode provided on rear plane of said semiconductor substrate,

a first metallic member connected to said first electrode, and

a second metallic member connected to said second electrode, wherein:

said second electrode is connected to said second metallic member via a metallic layer containing precious metal , and

said metallic layer is an alloy layer having a solidus line temperature at least 400 ℃, which contains a precious metal as a main component.

15. A semiconductor device comprising:

a semiconductor substrate,

a semiconductor element which comprises;

a first electrode provided on front plane of said semiconductor substrate, and a second electrode

provided on rear plane of said semiconductor substrate,

a first metallic member connected to said first electrode, and

a second metallic member connected to said second electrode, wherein:

said first metallic member comprises plural portions extended from a portion having a bonding portion with said first electrode, and

respective of said plural portions comprises a surface portion for connecting with an external line.

16. A semiconductor device as claimed in any of claims 1 and 2, wherein:

said second electrode provided on the rear plane of said semiconductor substrate is formed by metalizing said semiconductor substrate after grinding.

17. A semiconductor device as claimed in any of claims 1 and 2, wherein:

at least one of said first and second metallic bodie pads is composed of a solder having a melting point at least 250 ℃.

18. A method for manufacturing said semiconductor device claimed in claim 1, wherein:

a bonding operation for bonding said first electrode with said first metallic member of said semiconductor is performed simultaneously with or prior

to a bonding operation for bonding said second electrode with said second metallic member of said semiconductor.

19. A semiconductor device comprising:

a semiconductor chip, and

a metallic member connected to chip electrode, wherein:

said chip electrode is composed of any of Al film and an Al alloy film,

a bonding front plane of said metallic member is composed of plated precious metal film,

said chip electrode is bonded metallically to said metallic member via Au bumps, and

said Aluminum film of more than 80 % in area of Au/Al bonding region is made all an Au/Al alloy layer in the thickness direction.

20. A semiconductor device comprising:

a semiconductor chip,

a first metallic member connected to chip rear plane electrode,

a second metallic member connected to a main current electrode on a circuit forming plane of the chip, and

a third metallic member connected to a control electrode, wherein:

said main current electrode and said control electrode are composed of any of Al film and an Al alloy film,

plural Au bumps are formed on respective of Al electrode film in a metallically bonded condition,

respective of said second and third metallic members, which is plated with precious metal , has such a structure that said metallic member is bonded with said Au bumps by compression bonding, and gaps between said metallic member and said chip are filled with resin, and

a plane of said first metallic member opposite to said chip in the plane of chip projection, and planes of said second and third metallic members opposite to said chip are exposed to the surface of said semiconductor device.

21. A semiconductor device comprising:

a semiconductor chip, and

a metallic member connected to chip electrode, wherein:

precious metal particles, having a particle diameter larger than a gap between said chip and said metallic member, and resin are filled into said gap, and

such a structure is composed that precious metal bumps, having a bump diameter larger than said gap between said chip and said metallic member, and resin are filled into said gap between said chip and said metallic member.

22. A semiconductor device as claimed in claim 21, wherein:

respective of said precious metal particles, said

metallic member, and said electrode; and said precious metal bumps, said metallic member, and said electrode; are bonded metallically each other.

23. A semiconductor device comprising:

a semiconductor chip, and

metallic members connected to chip electrodes, wherein:

main mechanical bonding between said metallic members are performed via said chip.

24. A semiconductor device comprising:

a semiconductor chip,

metallic members connected to chip electrodes, and

resin filled into a gap between said chip and said metallic members, wherein:

said metallic member is manufactured to have any of bumps and dips, and openings, for composing a mechanically bonded structure with said resin.

Abstract of the disclosure

A semiconductor device, wherein a first metallic member is bonded to a first electrode of semiconductor element via a first metallic body containing first precious metal , and a second metallic member is bonded to a second electrode via a second metallic body containing second precious metal .

FIG. 1

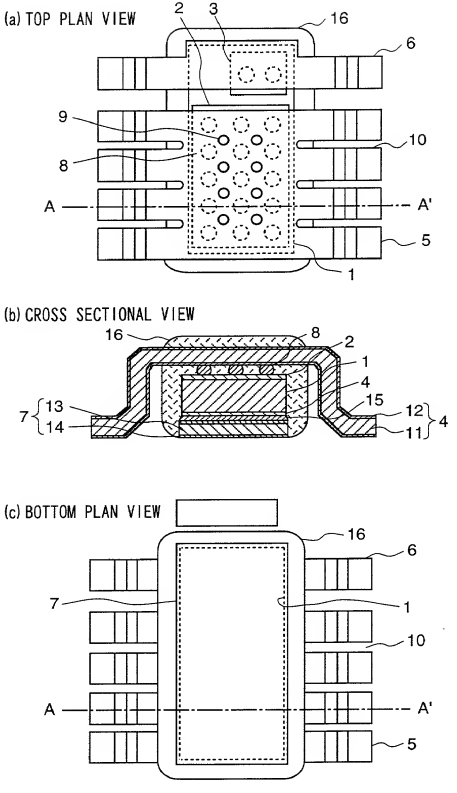

(a) TOP PLAN VIEW
2
3
16
6
9
10
8
A
A'
5
1
(b) CROSS SECTIONAL VIEW
16
8
2
1
4
15
12
11
4
7
13
14
(c) BOTTOM PLAN VIEW
16
6
7
1
10
A
A'
5

FIG. 2

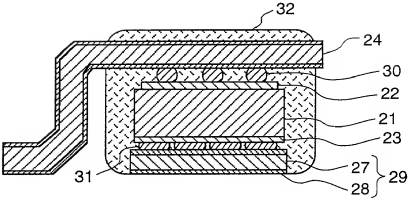


FIG. 3

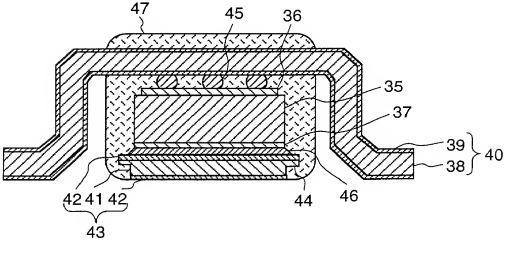
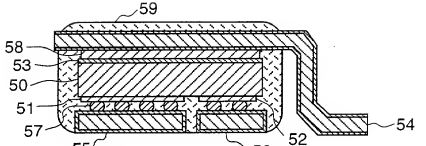
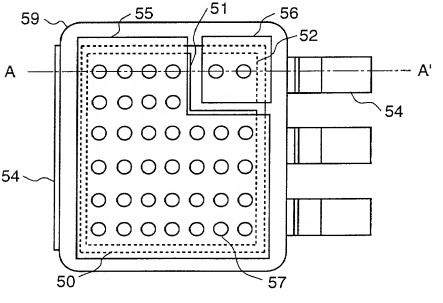


FIG. 4



(b) CROSS SECTIONAL VIEW



(c) BOTTOM PLAN VIEW

FIG. 5

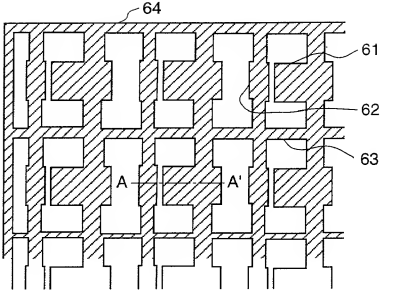


FIG. 6

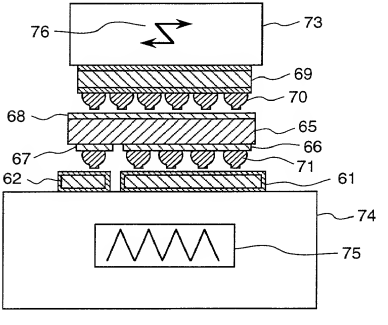


FIG. 7

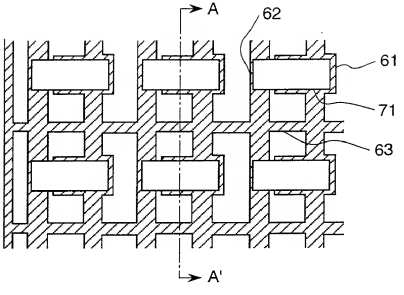


FIG. 8

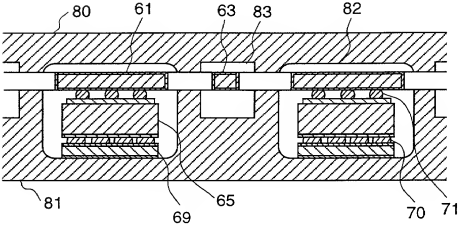


FIG. 9

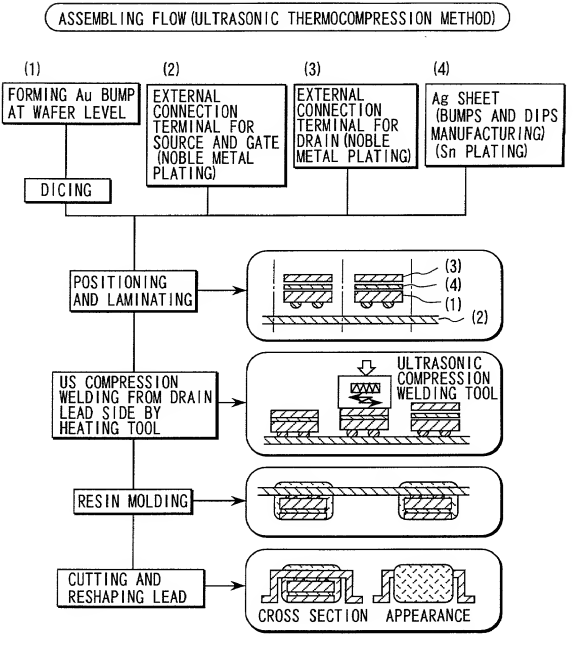
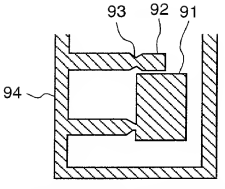
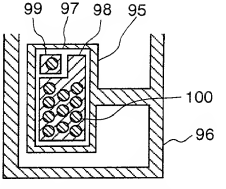

ASSEMBLING FLOW (ULTRASONIC THERMOCOMPRESSION METHOD)
(1)
FORMING Au BUMP AT WAFER LEVEL
DICING
(2)
EXTERNAL CONNECTION TERMINAL FOR SOURCE AND GATE (NOBLE METAL PLATING)
(3)
EXTERNAL CONNECTION TERMINAL FOR DRAIN (NOBLE METAL PLATING)
(4)
Ag SHEET (BUMPS AND DIPS MANUFACTURING) (Sn PLATING)
POSITIONING AND LAMINATING
(3)
(4)
(1)
(2)
US COMPRESSION WELDING FROM DRAIN LEAD SIDE BY HEATING TOOL
ULTRASONIC COMPRESSION WELDING TOOL
RESIN MOLDING
CUTTING AND RESHAPING LEAD
CROSS SECTION APPEARANCE

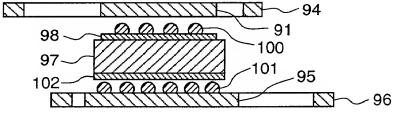
FIG. 10



(a) LEAD FRAME FOR SOURCE/GATE

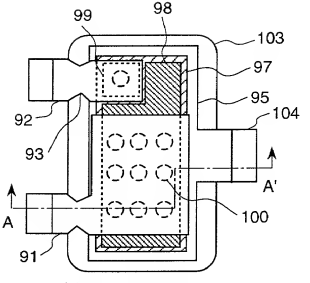


(b) LEAD FRAME FOR DRAIN

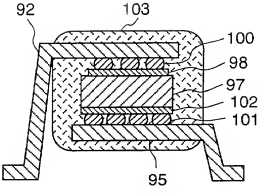


(c) LAMINATED CROSS SECTIONAL STRUCTURE AT BONDING

FIG. 11

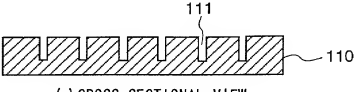


(a) TOP PLAN VIEW

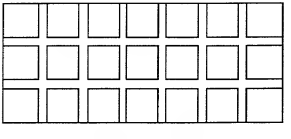


(b) A-A' CROSS SECTION

FIG. 12



(a) CROSS SECTIONAL VIEW

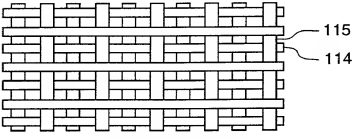


(b) TOP PLAN VIEW

FIG. 13

FIG. 14

(A) CROSS SECTION



(b) TOP PLAN VIEW

FIG. 15

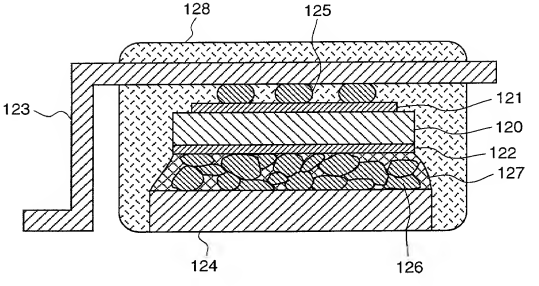

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FIG. 16

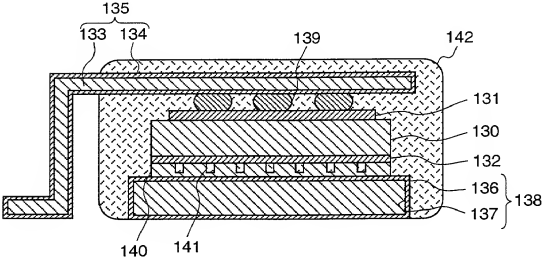
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FIG. 17

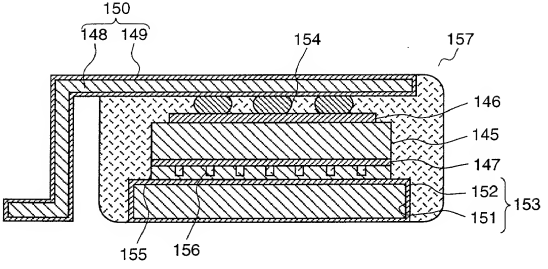
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FIG. 18

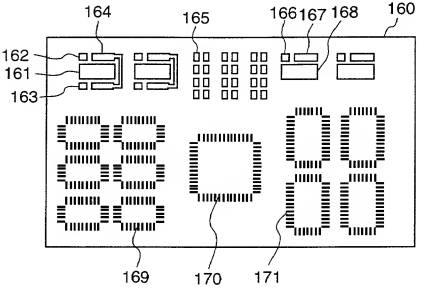
164
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FIG. 19

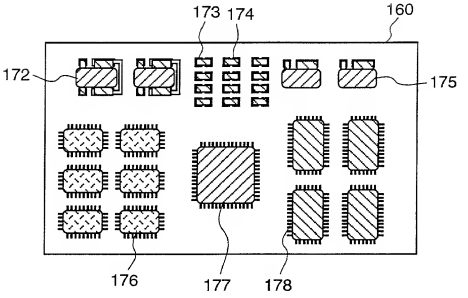
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FIG. 20

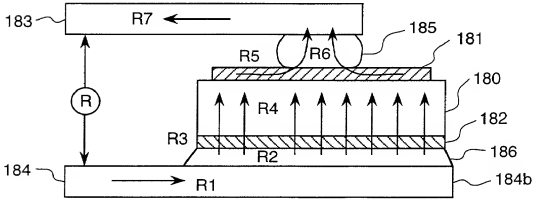
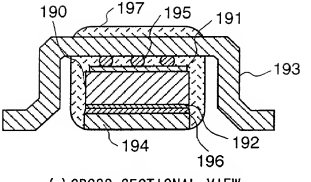
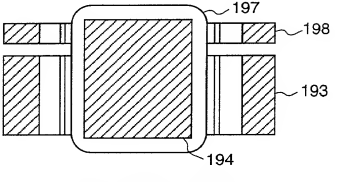

183
R7
185
181
R5
R6
180
R
R4
182
R3
186
R2
184
R1
184b

FIG. 21

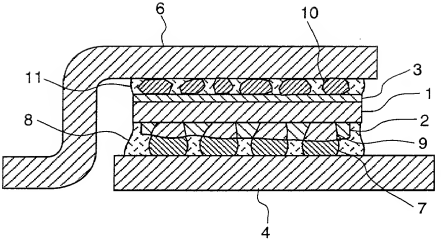


(a) CROSS SECTIONAL VIEW

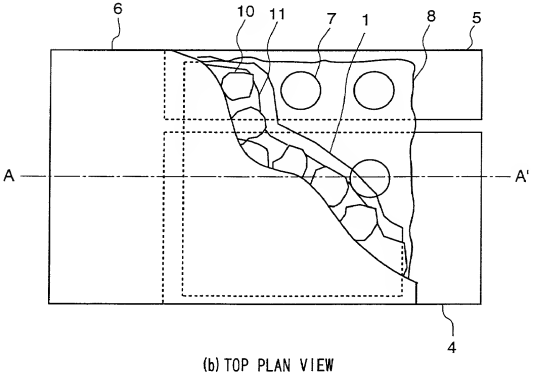


(b) BOTTOM PLAN VIEW

FIG. 22



(a) A-A' CROSS SECTIONAL VIEW



(b) TOP PLAN VIEW

FIG. 23

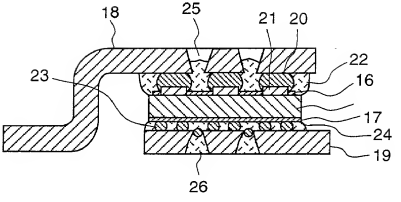

18
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FIG. 24

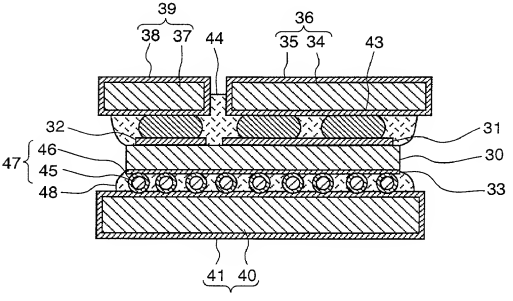
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FIG.25

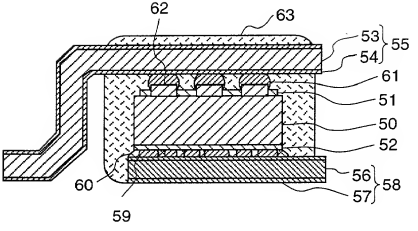


FIG.26

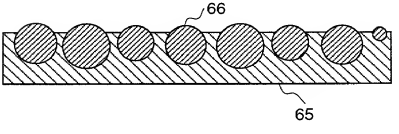


FIG.27

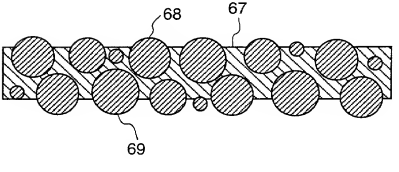


FIG. 28(a)

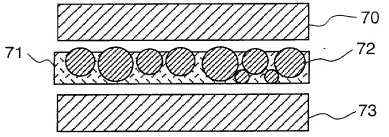


FIG. 28(b)

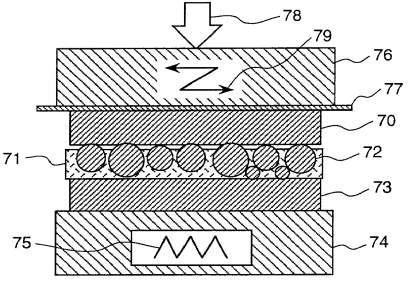


FIG. 28(c)

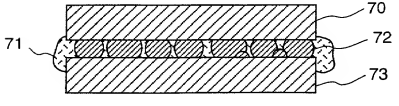


FIG. 29

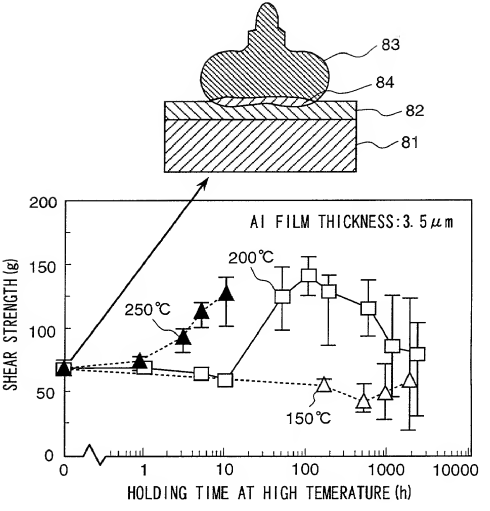

83
84
82
81
Al FILM THICKNESS:3.5μm
200℃
250℃
150℃
SHEAR STRENGTH (g)
HOLDING TIME AT HIGH TEMERATURE (h)
200
150
100
50
0
0
1
10
100
1000
10000

FIG. 30

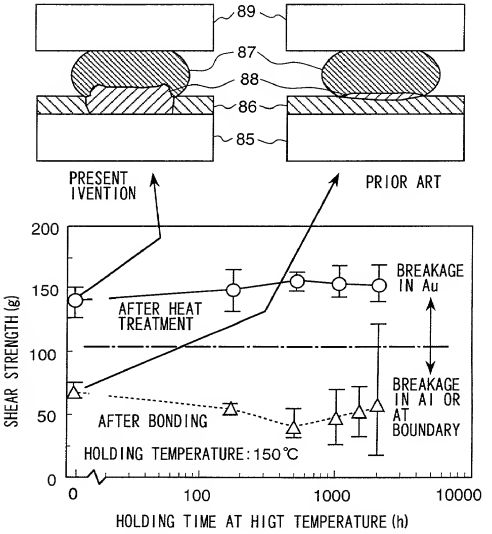
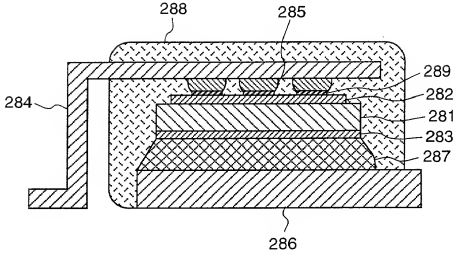

89
87
88
86
85
PRESENT IVENTION
PRIOR ART
200
150
100
50
0
SHEAR STRENGTH (g)
BREAKAGE IN Au
AFTER HEAT TREATMENT
BREAKAGE IN Al OR AT BOUNDARY
AFTER BONDING
HOLDING TEMPERATURE: 150℃
0
100
1000
10000
HOLDING TIME AT HIGT TEMPERATURE (h)

FIG. 31


288
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286

FIG. 32

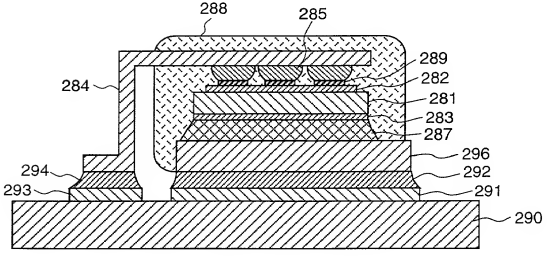
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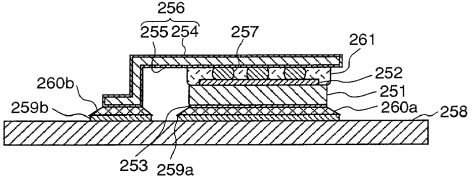
FIG. 33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255
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260a
258
260b
259b
253
259a

FIG. 34

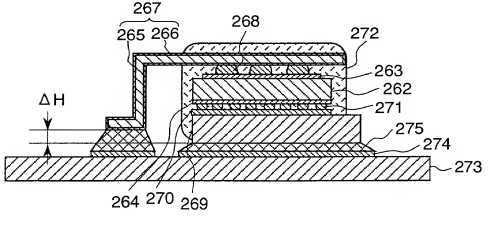

267
265
266
268
272
263
262
271
275
274
273
ΔH
264
270
269

FIG. 35(a)

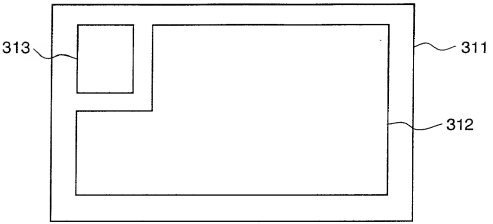
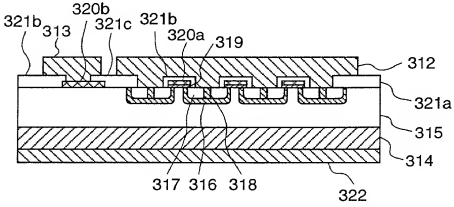


FIG. 35(b)



DECLARATION AND POWER OF ATTORNEY FOR PATENT APPLICATION

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name, I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled:

SEMICONDUCTOR DEVICE

the specification of which (check one)

[X] is attached hereto.

[ ] was filed on _____
as Application Serial No. _____
and was amended on _____ .
(if applicable)

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose information which is material to the examination of this application in accordance with Title 37, Code of Federal Regulations, §1.56(a).

I, hereby claim foreign priority benefits under Title 35, United States Code, §119 of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed:

Prior Foreign Application(s)			Priority Claimed	
11-19431	Japan	28/01/1999	[X] Yes	[ ] No
(Number)	(Country)	(Day/Month/Year Filed)		
11-160539	Japan	08/06/1999	[X] Yes	[ ] No
(Number)	(Country)	(Day/Month/Year Filed)		
(Number)	(Country)	(Day/Month/Year Filed)	[ ] Yes	[ ] No
(Number)	(Country)	(Day/Month/Year Filed)	[ ] Yes	[ ] No
(Number)	(Country)	(Day/Month/Year Filed)	[ ] Yes	[ ] No
(Number)	(Country)	(Day/Month/Year Filed)	[ ] Yes	[ ] No

I hereby claim the benefit under Title 35, United States Code, §120 of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, §112, I acknowledge the duty to disclose material information as defined in Title 37, Code of Federal Regulations, §1.56(a) which occurred between the filing date of the prior application and the national or PCT international filing date of this application:

(Application Serial No.)	(Filing Date)	(Status: patented, pending, abandoned)
(Application Serial No.)	(Filing Date)	(Status: patented, pending, abandoned)
(Application Serial No.)	(Filing Date)	(Status: patented, pending, abandoned)
(Application Serial No.)	(Filing Date)	(Status: patented, pending, abandoned)

(Continued on Page 2)

I hereby appoint as principal attorneys; Donald R. Antonelli, Reg. No. 20,296; David T. Terry, Reg. No. 20,178; Melvin Kraus, Reg. No. 22,466; Stanley A. Wal, Reg. No. 26,432; William I. Solomon, Reg. No. 28,565; Gregory E. Montone, Reg. No. 28,141; Ronald J. Shore, Reg. No. 28,577; Donald E. Stout, Reg. No. 26,422; Alan E. Schiavelli, Reg. No. 32,087; James N. Dresser, Reg. No. 22,973 and Carl I. Brundidge, Reg. No. 29,621 to prosecute and transact all business connected with this application and any related United States application and international applications. Please direct all communications to the following address:

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I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further, that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

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